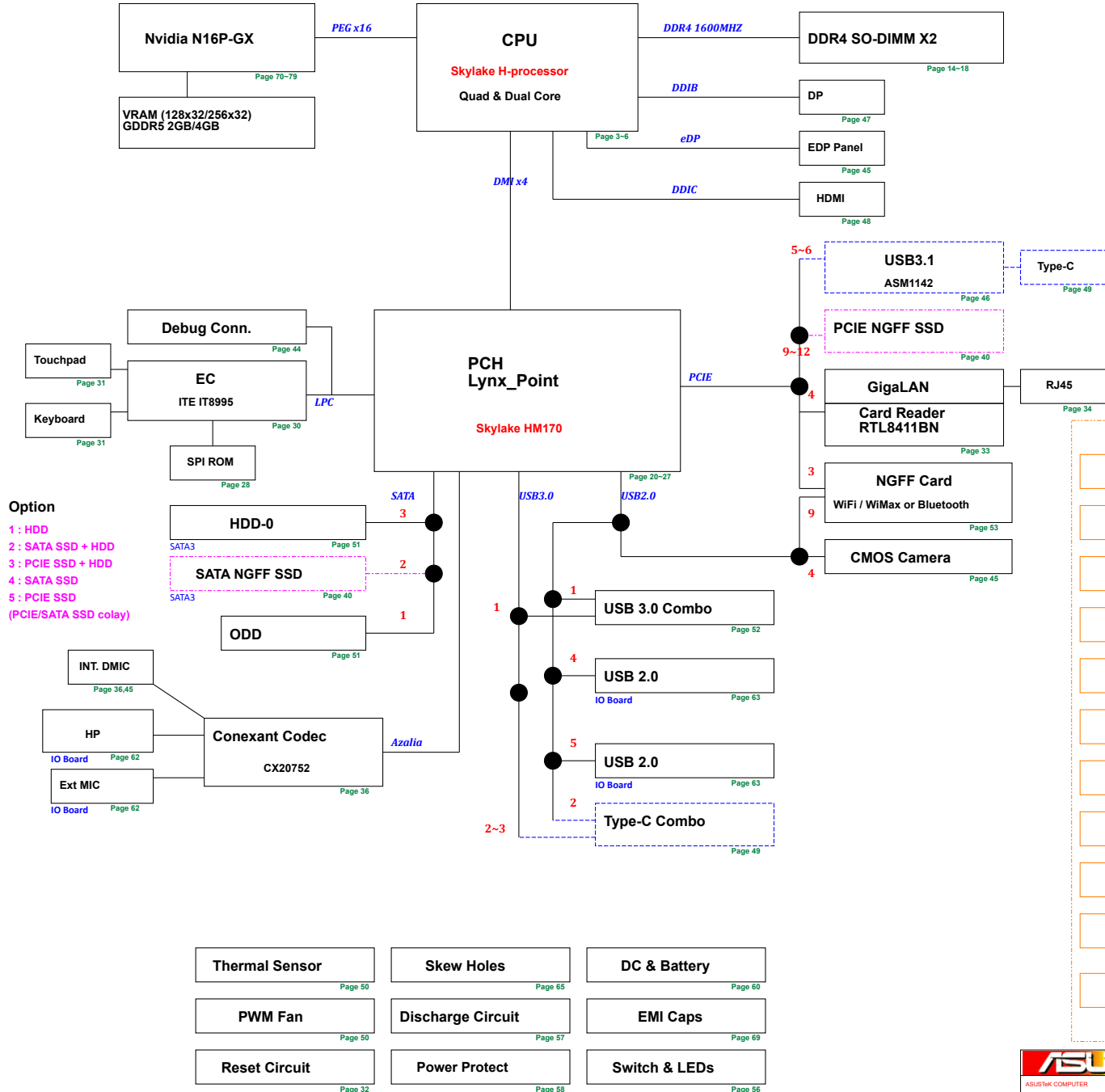


- 001_Block Diagram
002_System Setting
003_CPU_DMI,PEG,eDP,DDI
004_CPU_DDR4
005_CPU_GND
006_CPU_CFG,RSVD
007_CPU_XDP
008_CPU_PWR
009_CPU_PWR
010_CPU_POWER_CAP
014_DIM_DDR4 SO-DIMM A(0) TOP
015_DIM_DDR4 SO-DIMM B(0) TOP
018_DIM_CA/DQ Voltage
020_PCH_HDA,SMBUS,SYS PWR,JTAG
021_PCH-CPT(2)_PCIE,USB2,MISC
022_PCH-CPT(3)_CLK,LPC,USB3
023_PCH-CPT(4)_eDP,PCI,DP
024_PCH-CPT(5)_SPI
025_PCH-CPT(6)_GPIO
026_PCH-CPT(7)_POWER,GND
027_PCH-CPT(8)_POWER,GND
028_PCH-SPI ROM,OTH
029_PCH-XDP
030_KBC_IT8995
031_KBC_KB & TP
032_RST_Reset Circuit
033_LAN_CR_RTL8411BN
034_LAN RJ45
036-AUD-CX20752
037-AUD-AMP
038_AUD-SPEAKER Connector
040_NGFF_SSD
044_DEBUG_LPC
045_eDP
046_USB 3.1 ASM1142
047_DDI_miniDP
048_DDI_HDMI
049_USB 3.1 MB Type-C
050_FAN_Thermal Sensor & Fan
051_HDD & ODD CON
052_USB_Port
053_WiFi/WiMax
056_LED
057_DSG_Discharge
058_Power Protect
059_MB_to_I/O_CONN.
060_DC & BAT IN
062_>>>>>I/O board(1)_MIC/HP
063_>>>>>I/O board(2)_USB
064_>>>>>I/O board(3)_LID SW
065_ME_NUT
069_OTH_EMI
070_VGA_PCI-EXPRESS(1)
071_GPU_FB-IF_GDDR5(2)
072_FRAME BUFFER-A(3)
073_FRAME BUFFER-B(4)
074_VGA_CRT/LVDS(5)
075_VGA_GPIO/DVI/DP(6)
076_VGA_XTAL/STRAPPING(7)
077_VGA_PWG/GND(8)
078_VRAM Cap
080_PW_SKYLAKE (1)
081_PW_SKYLAKE (2)
083_PW_+1.0VSUS
086_PW_1.2V/+VTT/2.5V
087_PW_+3VADSW/+5VSUS
088_PW_LOAD SWITCH
089_PW_CHARGER
090_PW_PROTECTION
091_PW_+NVVDD
092_PW_+PEX_VDD
093_PW_+FBVDDQ

GL752VW Block Diagram

Skylake Platform



[illegible]

G751VW Setting			
SM-Box ADDRESS :			
PCB Header			
SM-Box Service	SM-Box Address		
SG-CONTR-ACU	15A		
SG-CONTR-ACU	15B		
SG-CONTR-ACU	15C		
SG-CONTR-ACU	15D		
EC-Header (SM&L)	SM-Box Address		
SM-Box Service			
WGS-Variable Address	05A		
WGS-Variable Address	05B		
Device Identification			
GV-Device Name			
Net	18000222010	NetType	
Net			

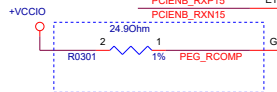
SkyLake HMMIO			
MMIO	MMIO Capabilities	Function	SRX
000	POWER FROM SPI2	GPIO	SRX0
01	GPIOIN0	GPIOB_IO	SRX0, SRX1
02	GPIOIN0 / GPIOIN1		SRX0, SRX1
03	GPIOIN0 / GPIOIN2		SRX0, SRX1
04	GPIOIN0A		SRX0, SRX1
05	GPIOIN0B	GPIOB_IO	SRX0, SRX1
06	GPIOIN0C		SRX0, SRX1
07	GPIOIN0D / GPIOIN0E		SRX0, SRX1
08	GPIOIN0F / GPIOIN0G		SRX0, SRX1
09	PCIOIN0	IOAPIC	SRX0
10	PCIOIN0 / GSE	IOAPIC / Configurable	SRX0
11	PCIOIN0 / GSE	IOAPIC	SRX0, SRX1
12	PCIOIN0B	IOAPIC 3.1	SRX0
13	PCIOIN0C		
14	PCIOIN0D		
15	PCIOIN0E / GPIOIN0F / GSE		
16	PCIOIN0F / GPIOIN0G		
17	PCIOIN0G	PCIOIN0 / IOAPIC	SRX0

19	POBRL/J /GB	1x H00	
20	POBRL/L /GBM41	000	
21	POBRL/L /GBM42	545x 020	
22	POBRL/L /GBM43		
23			
24			
25			
26			

[illegible]

EDS 544924
table 2-17

R0.1-25



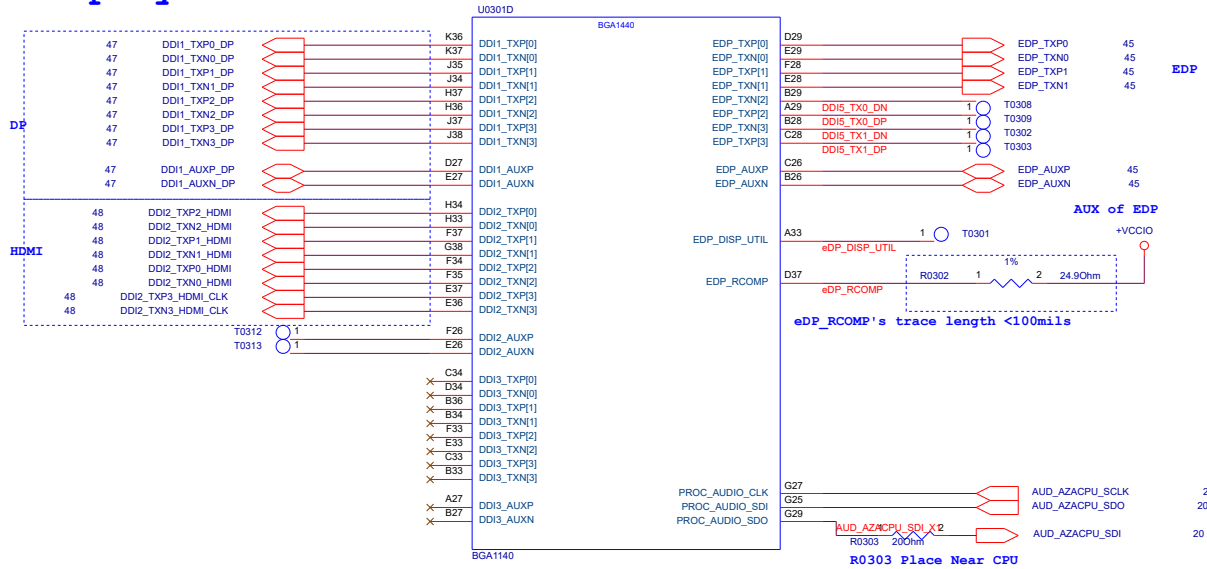
R0301 close to CPU
PEG_COMP trace length <400mils

R0.1-25

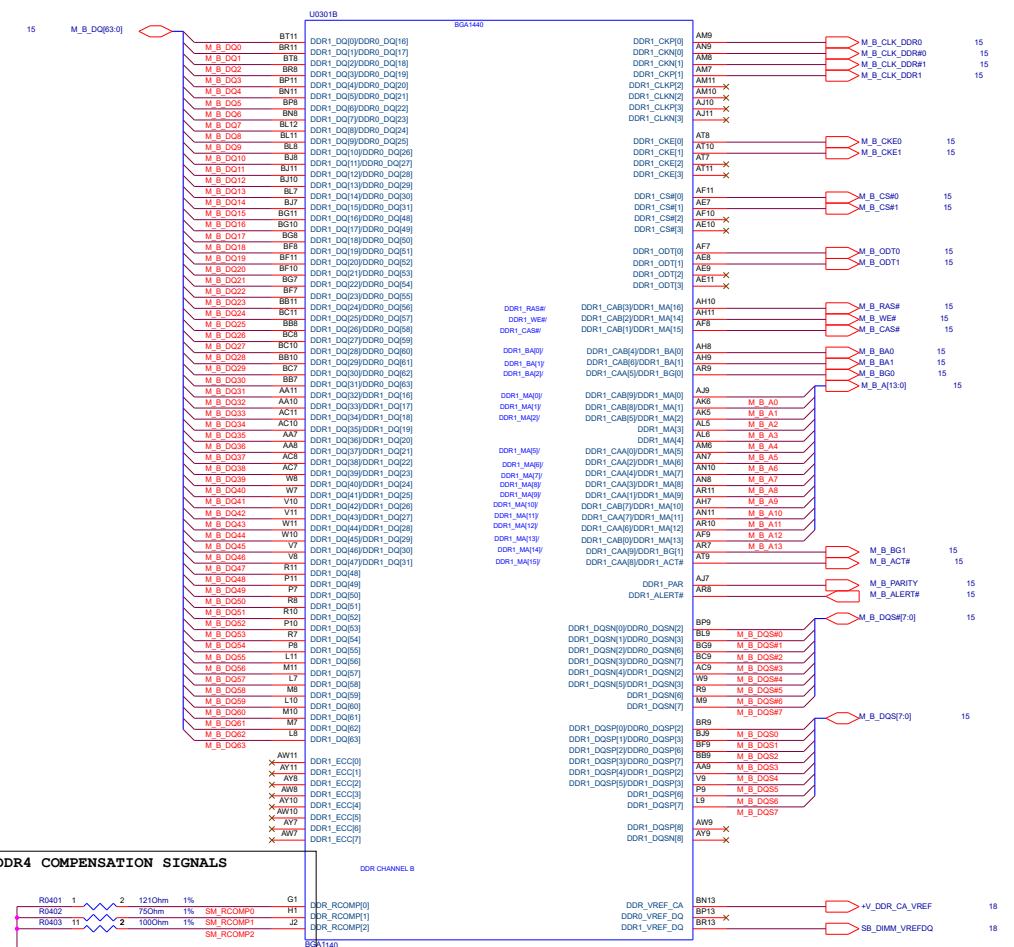
CFG2=0 -> Reversed
CFG5=0 -> PCIEG 2x8

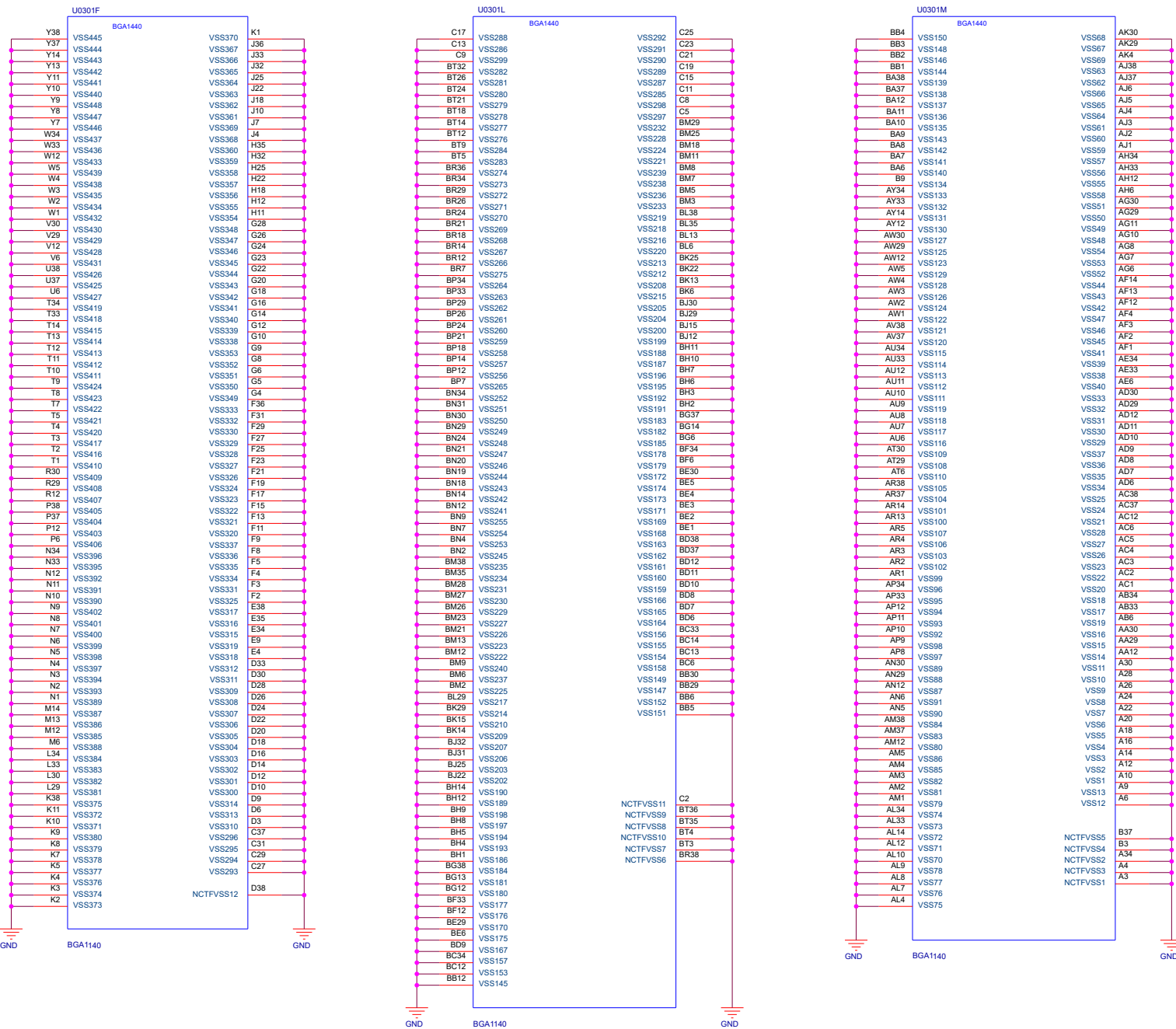
PCIEB_TXN8	CX0309	1	2	0.22UF/6.3V	PCIEG_RXN7
PCIEB_TXN9	CX0310	1	2	0.22UF/6.3V	PCIEG_RXN6
PCIEB_TXN10	CX0311	1	2	0.22UF/6.3V	PCIEG_RXN5
PCIEB_TXN11	CX0312	1	2	0.22UF/6.3V	PCIEG_RXN4
PCIEB_TXN12	CX0313	1	2	0.22UF/6.3V	PCIEG_RXN3
PCIEB_TXN13	CX0314	1	2	0.22UF/6.3V	PCIEG_RXN2
PCIEB_TXN14	CX0315	1	2	0.22UF/6.3V	PCIEG_RXN1
PCIEB_TXN15	CX0316	1	2	0.22UF/6.3V	PCIEG_RXN0
PCIEB_TXP8	CX0325	1	2	0.22UF/6.3V	PCIEG_RXP7
PCIEB_TXP9	CX0326	1	2	0.22UF/6.3V	PCIEG_RXP6
PCIEB_TXP10	CX0327	1	2	0.22UF/6.3V	PCIEG_RXP5
PCIEB_TXP11	CX0328	1	2	0.22UF/6.3V	PCIEG_RXP4
PCIEB_TXP12	CX0329	1	2	0.22UF/6.3V	PCIEG_RXP3
PCIEB_TXP13	CX0330	1	2	0.22UF/6.3V	PCIEG_RXP2
PCIEB_TXP14	CX0331	1	2	0.22UF/6.3V	PCIEG_RXP1
PCIEB_TXP15	CX0332	1	2	0.22UF/6.3V	PCIEG_RXP0

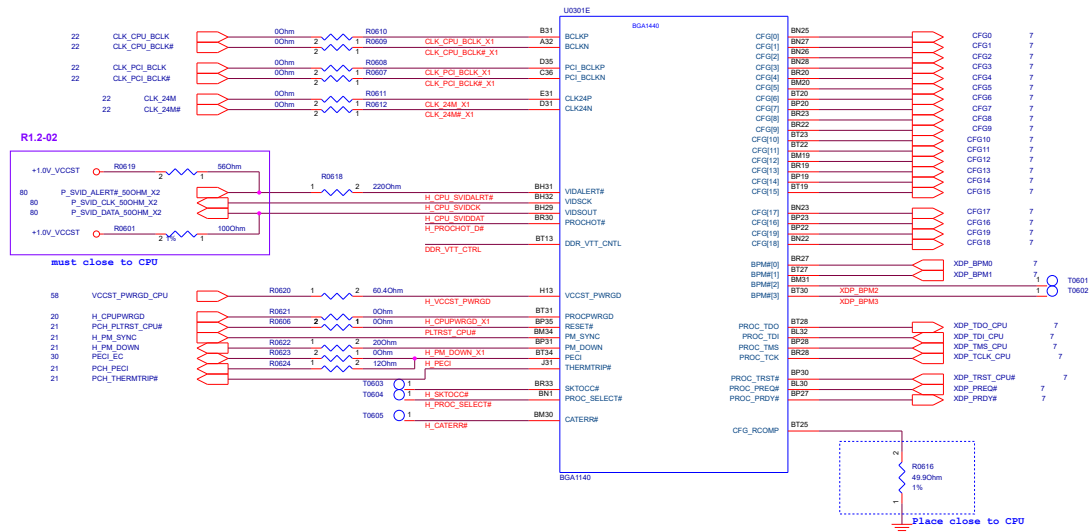
Display



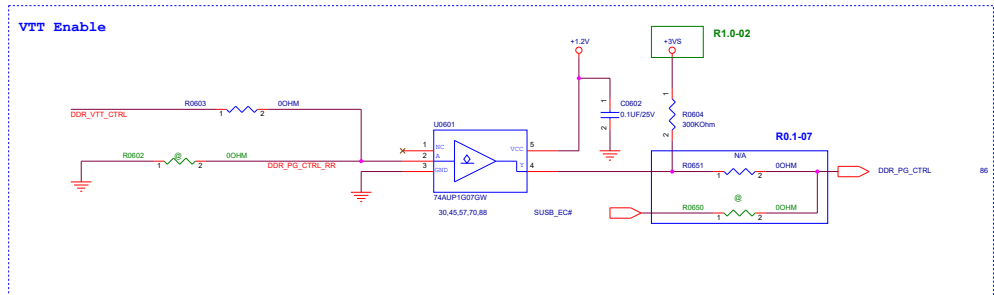
Main Board



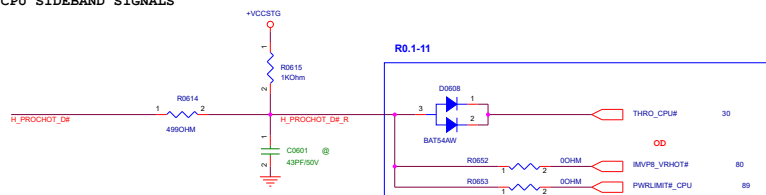




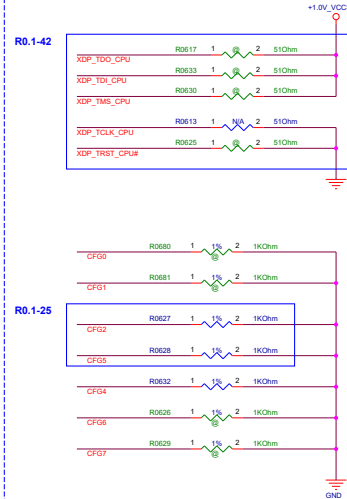
DDR_VTT_CTRL:
System Memory Power Gate Control:
Disables the platform memory VTT regulator
in C8 and deeper and S3.
Ref:544924_544924_Skylake_EDS_Vol_1_Rev0.9.pdf P.120



CPU SIDEBAND SIGNALS



CFG Straps



CFG Straps for Processor

ref : Intel 544924_Skylake_EDS_Vol_1_Rev0.9 P.121

CFG[0] : Stall reset sequence after PCU PLL lock until de-asserted
--

- 1 : (Default) Normal Operation; No stall
- 0 : Stall

CFG[1] : Reserved Configuration Lane

Reserved Configuration Lane

CFG[2] : PCI Express® Static x16 Lane Numbering Reversal

- 1 : (Default) Normal Operation
- 0 : Lane Numbers Reversed

CFG[3] : Reserved configuration lanes

Reserved Configuration Lane

CFG[4] : eDP Enable

- 1 : Disabled
- 0 : Enabled

CFG[6:5] : PCI Express® Bifurcation

- 00 : 1 x8 , 2 x4 PCI Express*
- 01 : Reserved
- 10 : 2 x8 PCI Express*
- 11 : 1 x16 PCI Express*

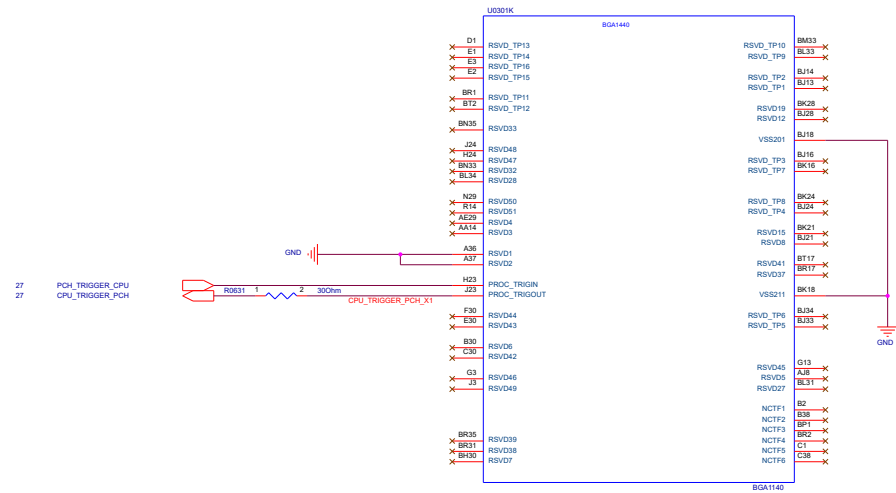
CFG[7] : PEG Training

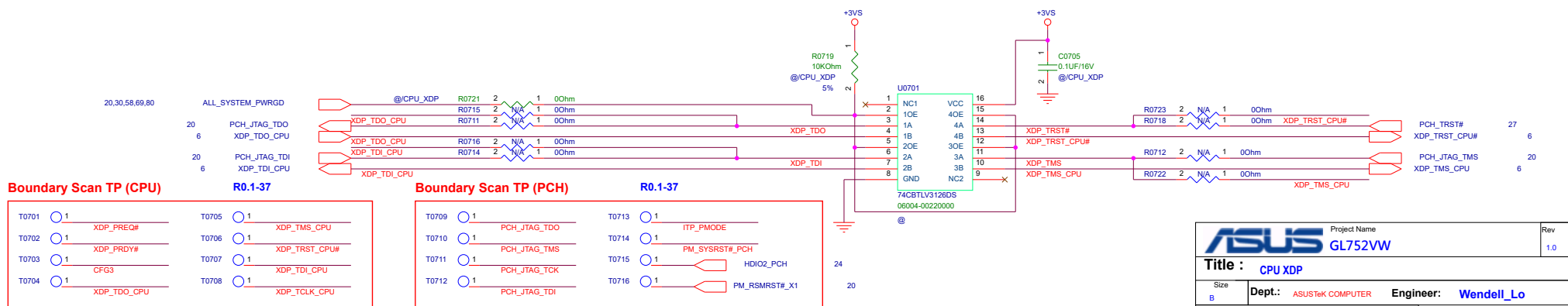
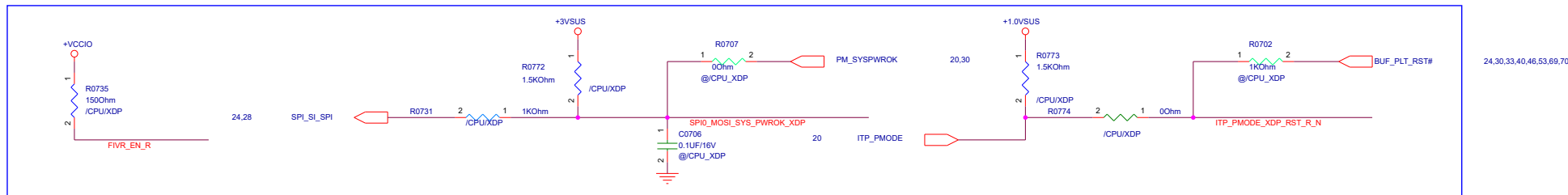
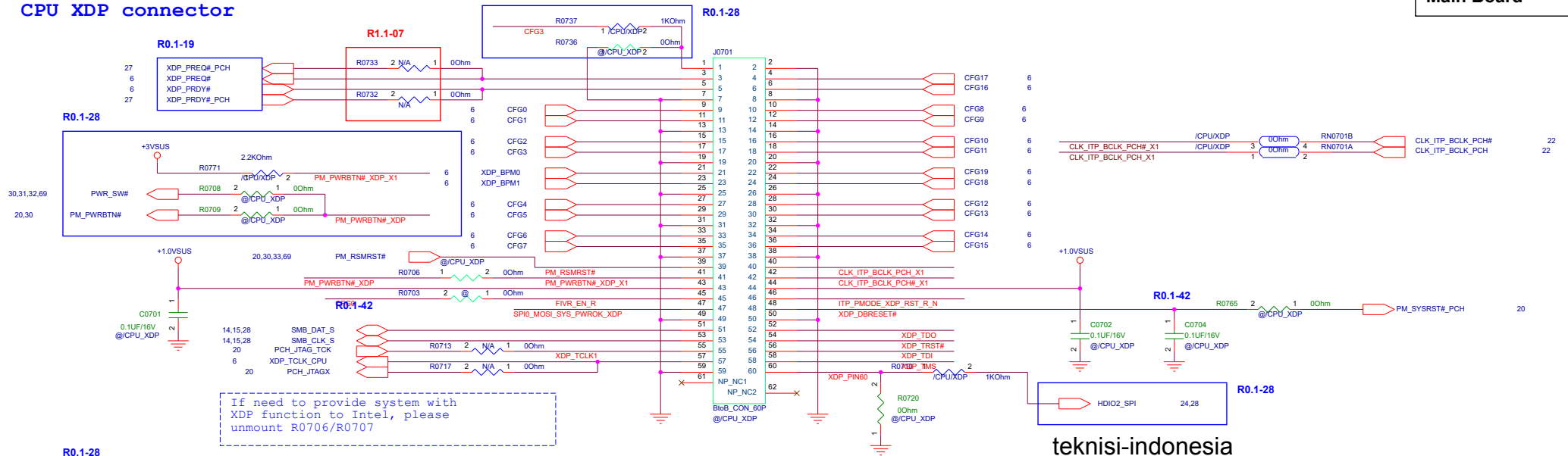
- 1 : (Default) PEG Train Immediately Following RESET# de-assertion
- 0 : PEG Wait for BIOS for Training

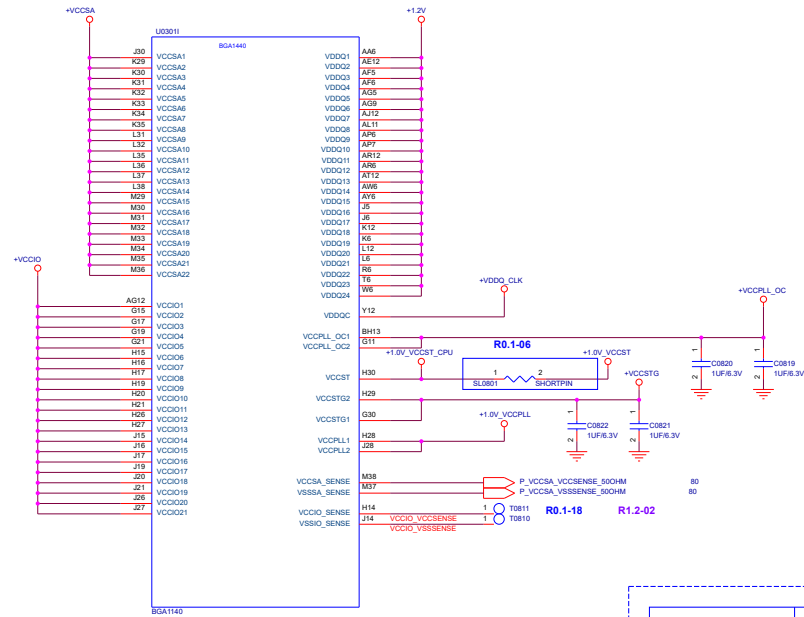
CFG[19:8] : Reserved Configuration Lanes

Reserved Configuration Lanes

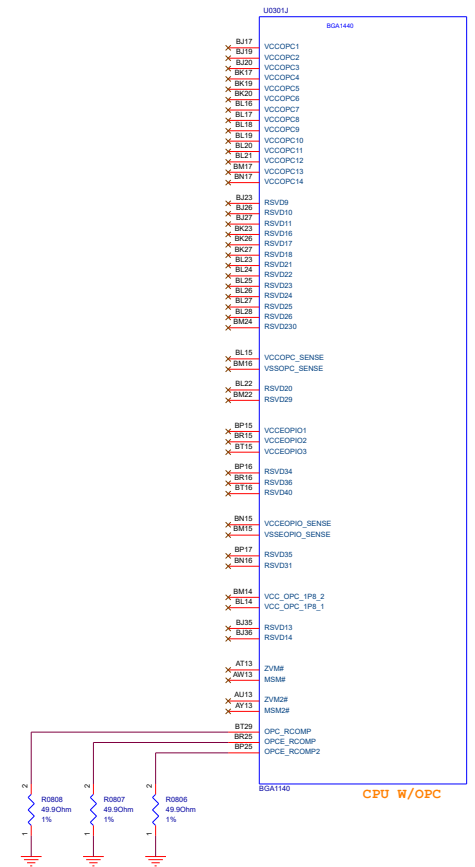
Intel 544924 Skylake_EDS_Vol_1_Rev0.9 P.121
Richard 20141209



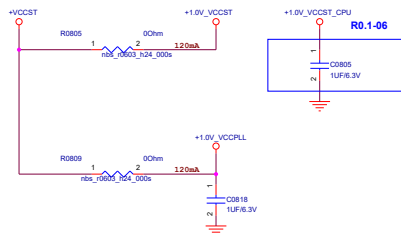




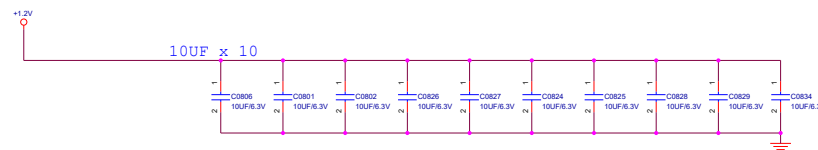
Main Source	1th PWR	2nd PWR	3rd PWR
AC_BAT_SYS	+1.0VSUS	+VCCST	+1.0V_VCCST
			+1.0V_VCCPLL
	+1.2V	+VDDQ_CPU +VCCPLL_OC	+VDDQ_CLK
	+VCCSA		
+VCCIO	+VCCSTG		



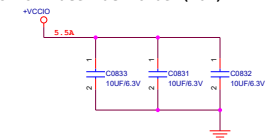
```
+1.0V VCCST/+1.0V VCCPLL
DECAPS Place Back Side (TOP)
```



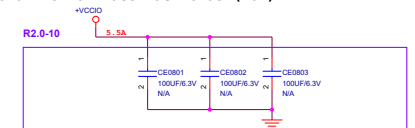
+VDDQ DECAPS Place Back Side (TOP)



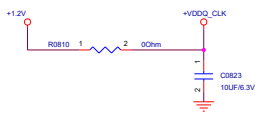
+VCCIO DECAPS Place Back Side (TOP)



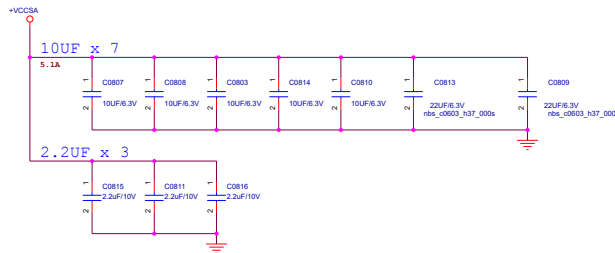
+VCCIO DECAPS Place Back Side (BOT)



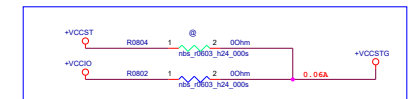
+VDDQ_CLK DECAPS Place Back Side (TOP)



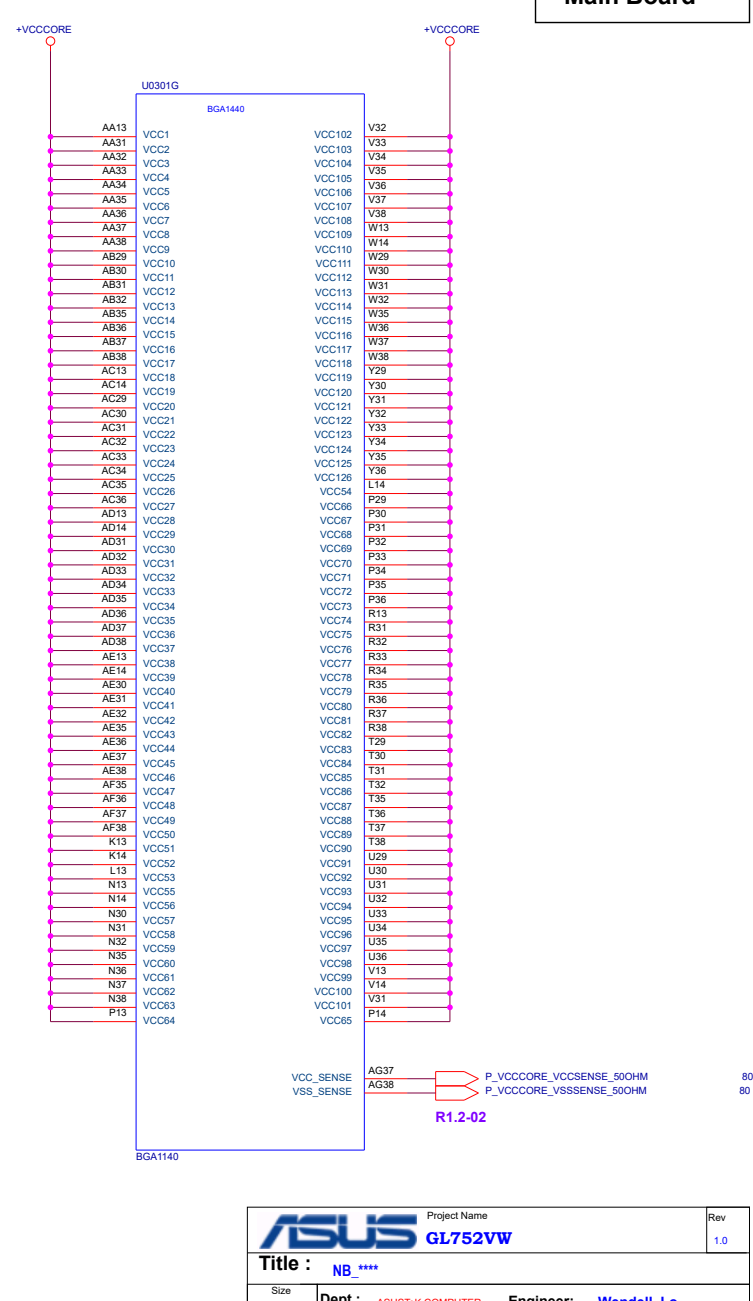
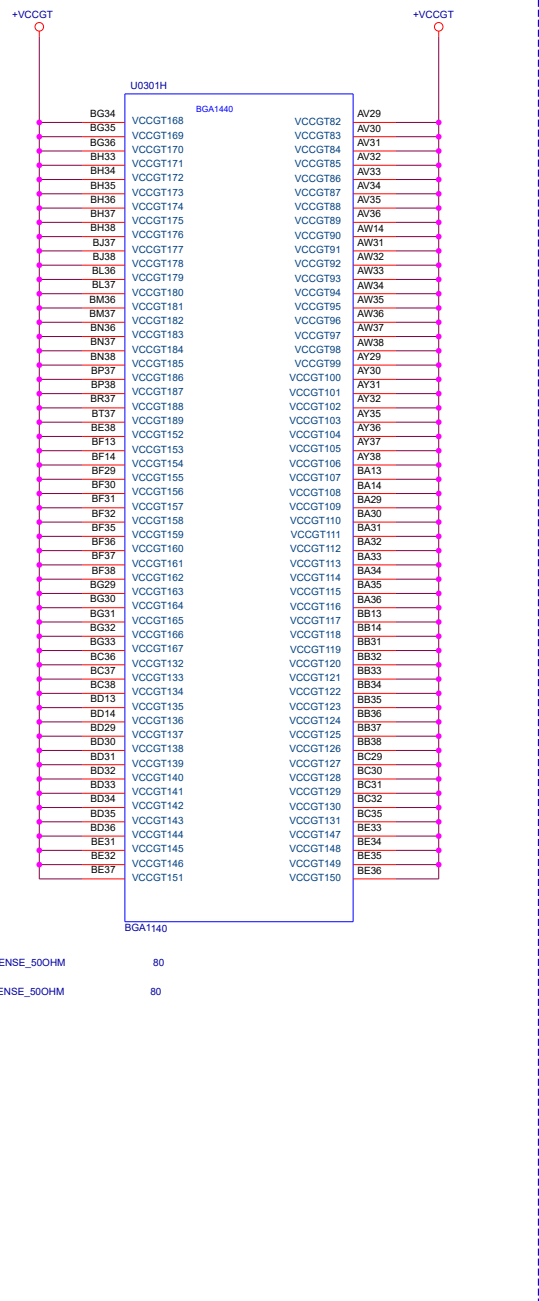
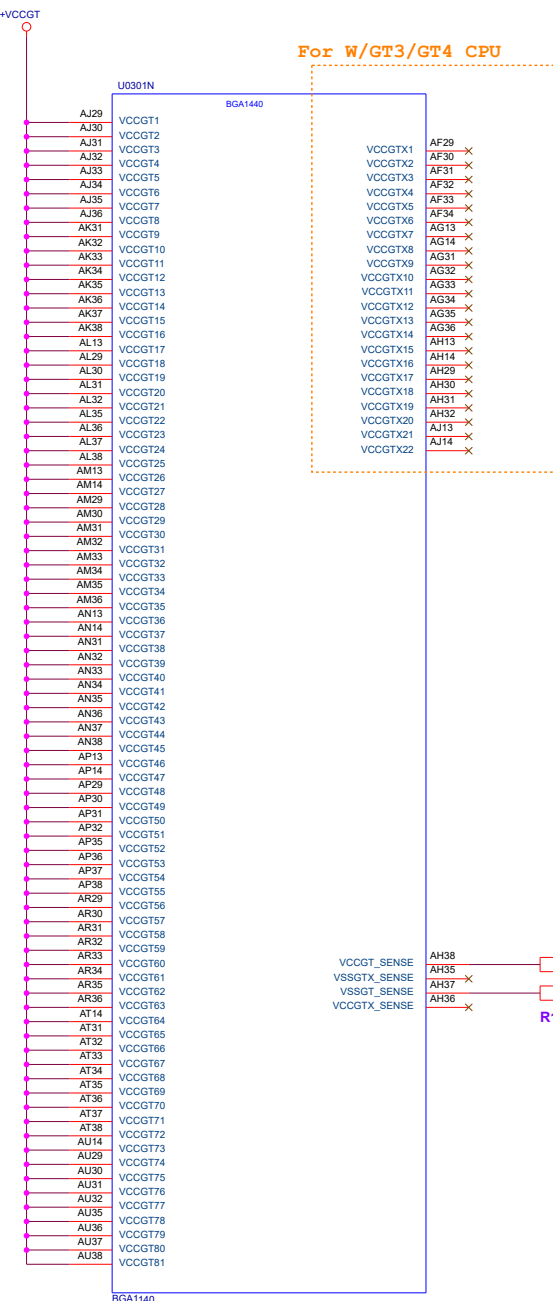
+VCCSA DECAPS Place Back Side (TOP)



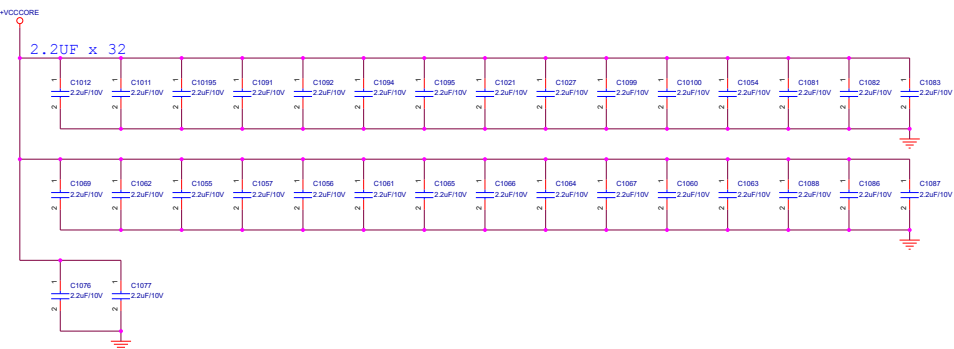
R0.1-06



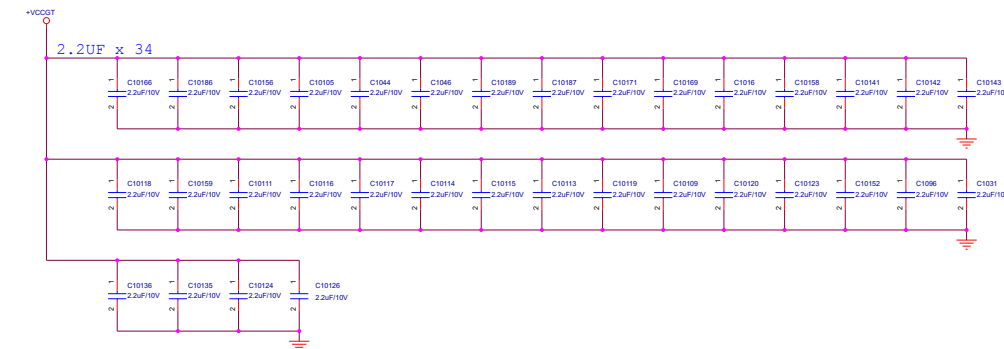
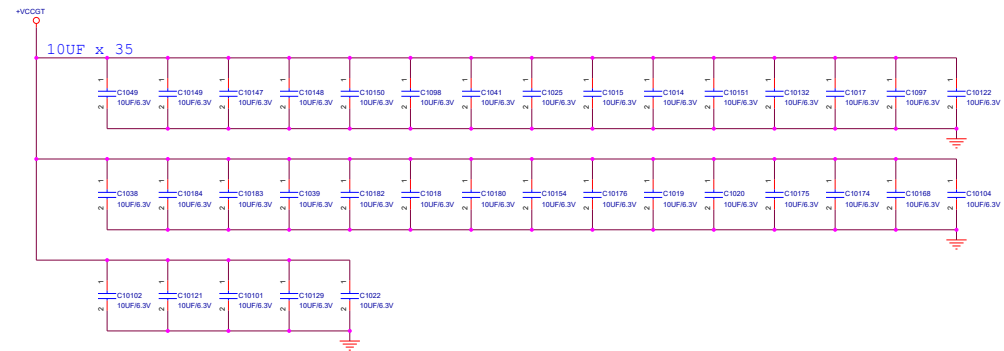
Volume Segment
+VCCIO is supplied +1.0VS (shared with +VCCSTG)



+VCCORE DECAPS Place Back Side (TOP)



+VCCGT DECAPS Place Back Side (TOP)



<Variant Name>

		Title : NB_****	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 11 of 102	

<Variant Name>

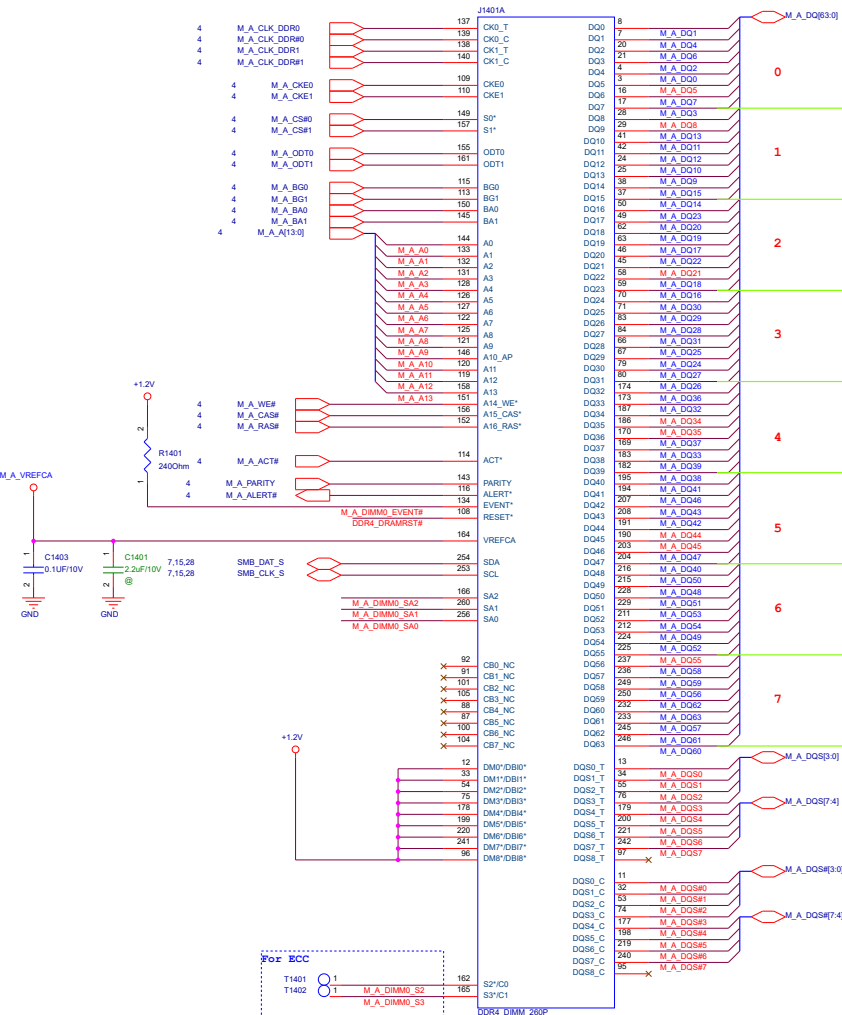
		Title : NB_****	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 12 of 102	

<Variant Name>

		Title : NB_****	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 13 of 102	

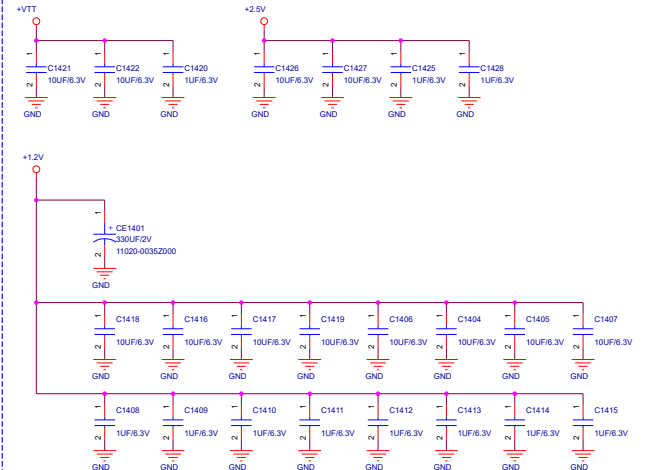
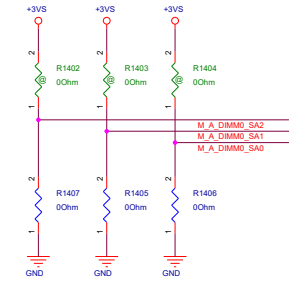
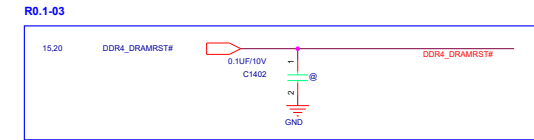
SODIMM CHA-DIMM0
TOP H4.0mm REV (J1401)

12002-00080600
DDR4 DIMM 260P 4H REV



SO-DIMMs that do not support ECC (x64 only) will use the SPD with EVENT# not wired. SO-DIMMs that support ECC (x72) will use a combined SPD/Thermal Sensor with EVENT# wired.

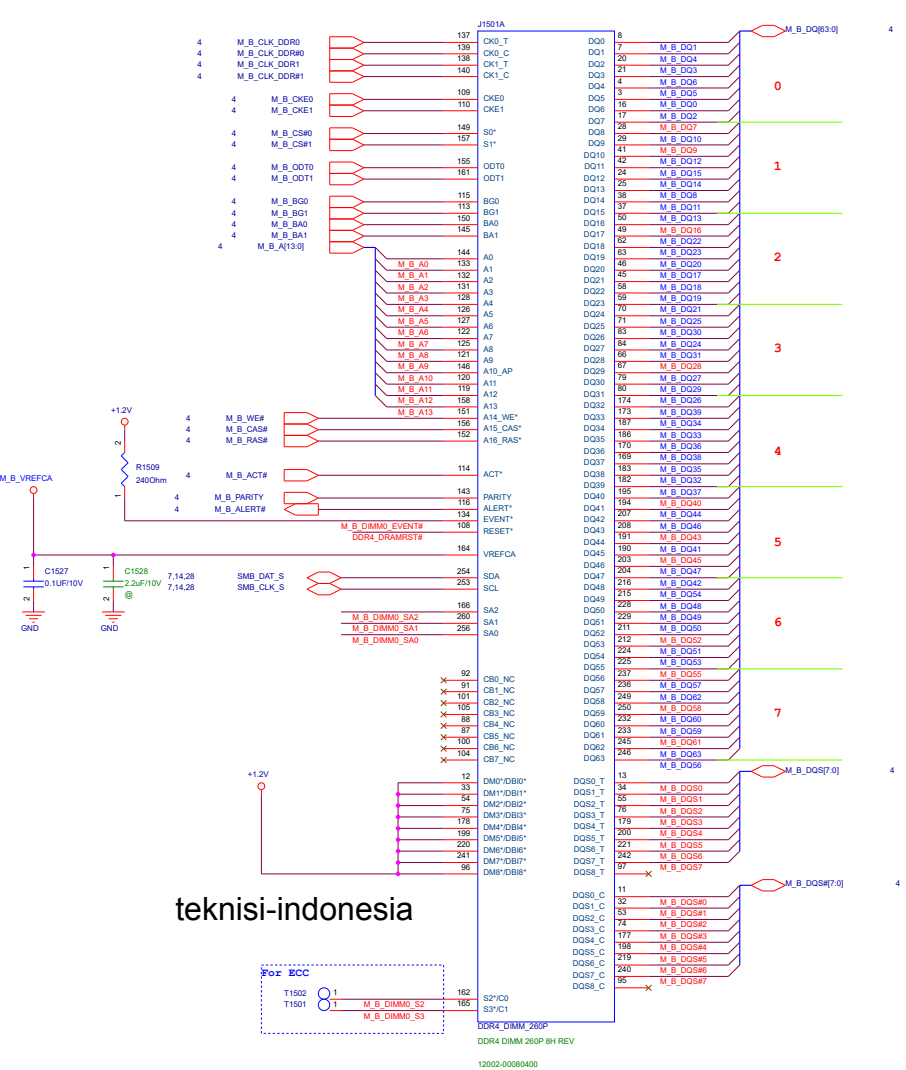
EVENT# ON ECC DIMM: KEEP A PULL UP IF NO PIN IN PCH



SODIMM CHB-DIMM0

TOP H8.0mm REV (J1501)

12002-00080400
DDR4 DIMM 260P 8H REV



<Variant Name>

		Title : NB_****	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 16 of 102	

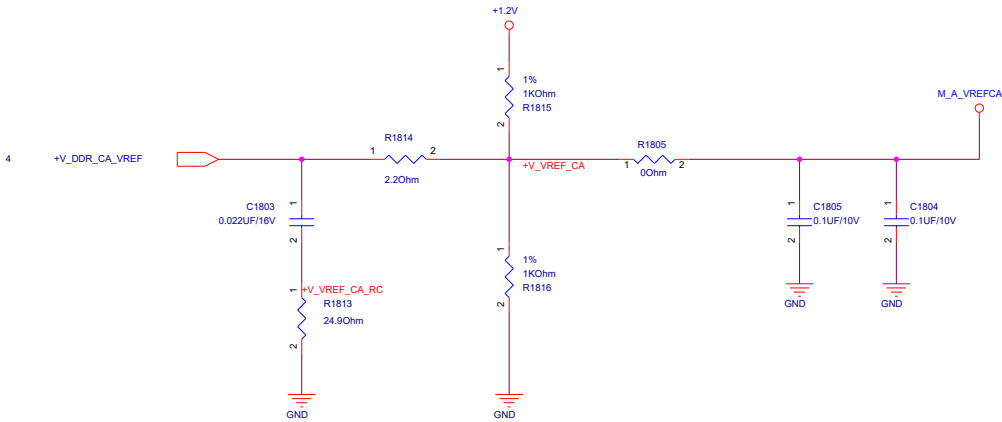
<Variant Name>

		Title : NB_****	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 17 of 102	

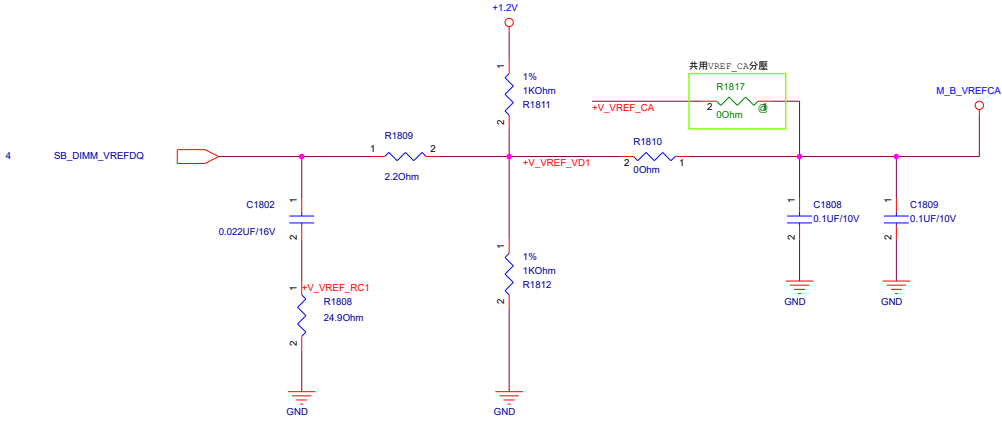
COMPRESSED
IMAGE

COMPRESSED
IMAGE

SO-DIMM0 Vref



SO-DIMM1 Vref



		Title : Green CLK Gen	
ASUSTek COMPUTER		Engineer: Wendell_Lo	
Size	Project Name	Rev	
A	GL752VW	1.0	
Date: Wednesday, September 23, 2015		Sheet	19 of 102

Main Board

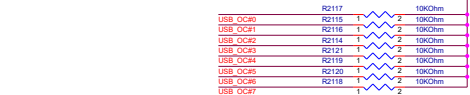
The diagram illustrates the ZU001C board and its connections to various storage devices. The top section shows the PCIe4 SSD, SATA SSD, and SATA HDD connections. The central section shows the ZU001C board with its various pins and connectors. The bottom section shows the PCIe4 SSD and SATA HDD connections.

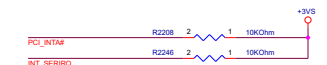
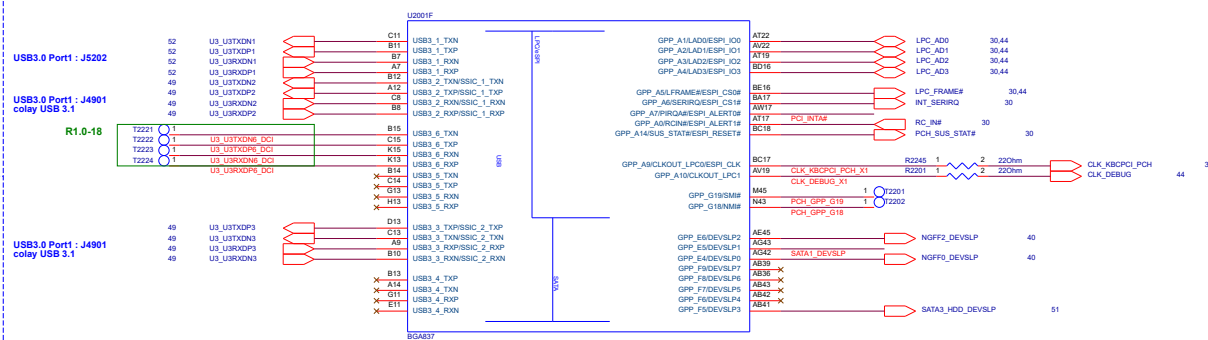
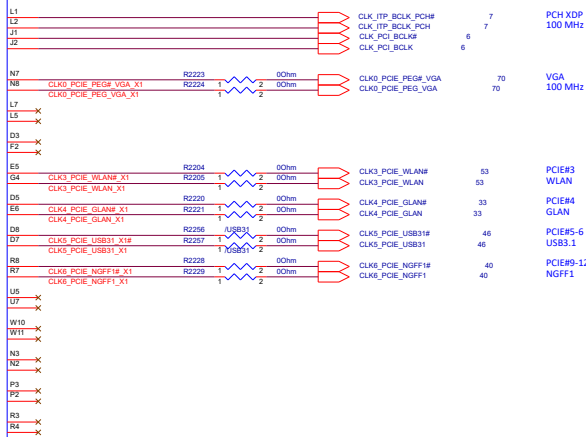
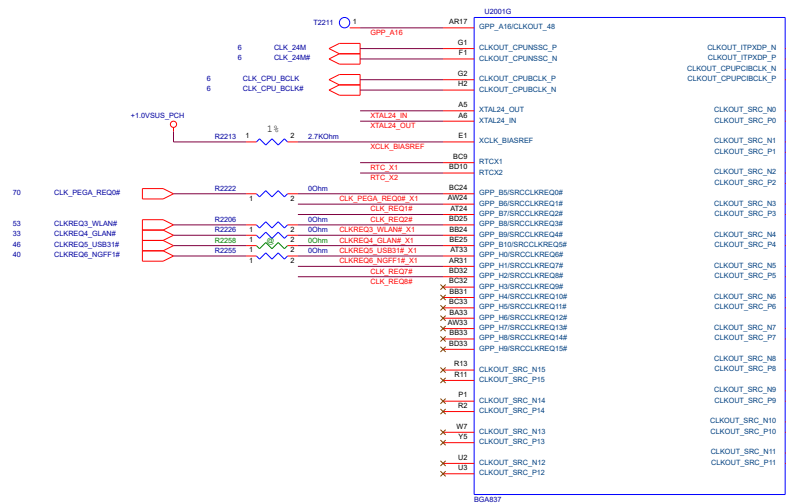
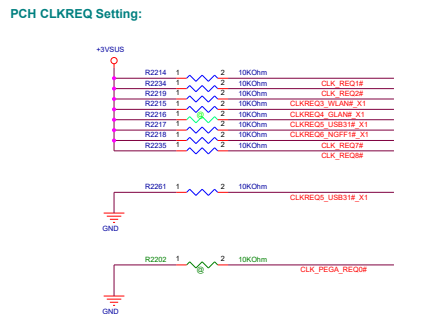
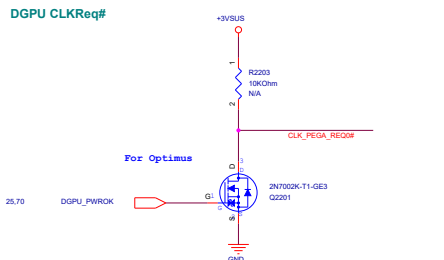
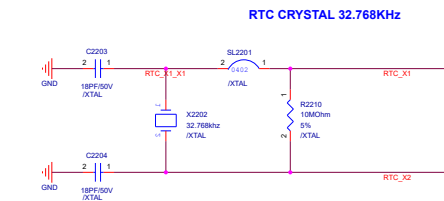
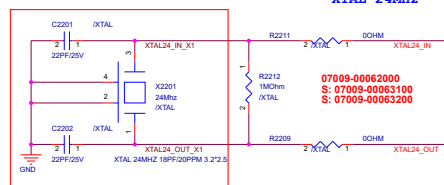
Top Section: Storage Connections

- PCIe4 SSD:**
 - PCIE11_TXP_NGFF1_L2 (40 pins)
 - PCIE11_TXP_NGFF1_L2 (40 pins)
 - PCIE11_TXP_NGFF1_L2 (40 pins)
- SATA SSD:**
 - SATA2_R0N_NGFF2_L0 (40 pins)
 - SATA2_R0P_NGFF2_L0 (40 pins)
 - SATA2_T0N_NGFF1_L1 (40 pins)
 - SATA2_T0P_NGFF1_L1 (40 pins)
- SATA HDD:**
 - SATA1_R0N_HDD (51 pins)
 - SATA1_R0P_HDD (51 pins)
 - SATA1_T0N_HDD (51 pins)
 - SATA1_T0P_HDD (51 pins)

Central Section: ZU001C Board

- Left Side (I/O):**
 - 21003 (1 pin)
 - 21004 (1 pin)
 - 21005 (1 pin)
 - 21006 (1 pin)
 - 21007 (1 pin)
 - 21008 (1 pin)
 - 21009 (1 pin)
 - 21010 (1 pin)
 - 21011 (1 pin)
 - 21012 (1 pin)
 - 21013 (1 pin)
 - 21014 (1 pin)
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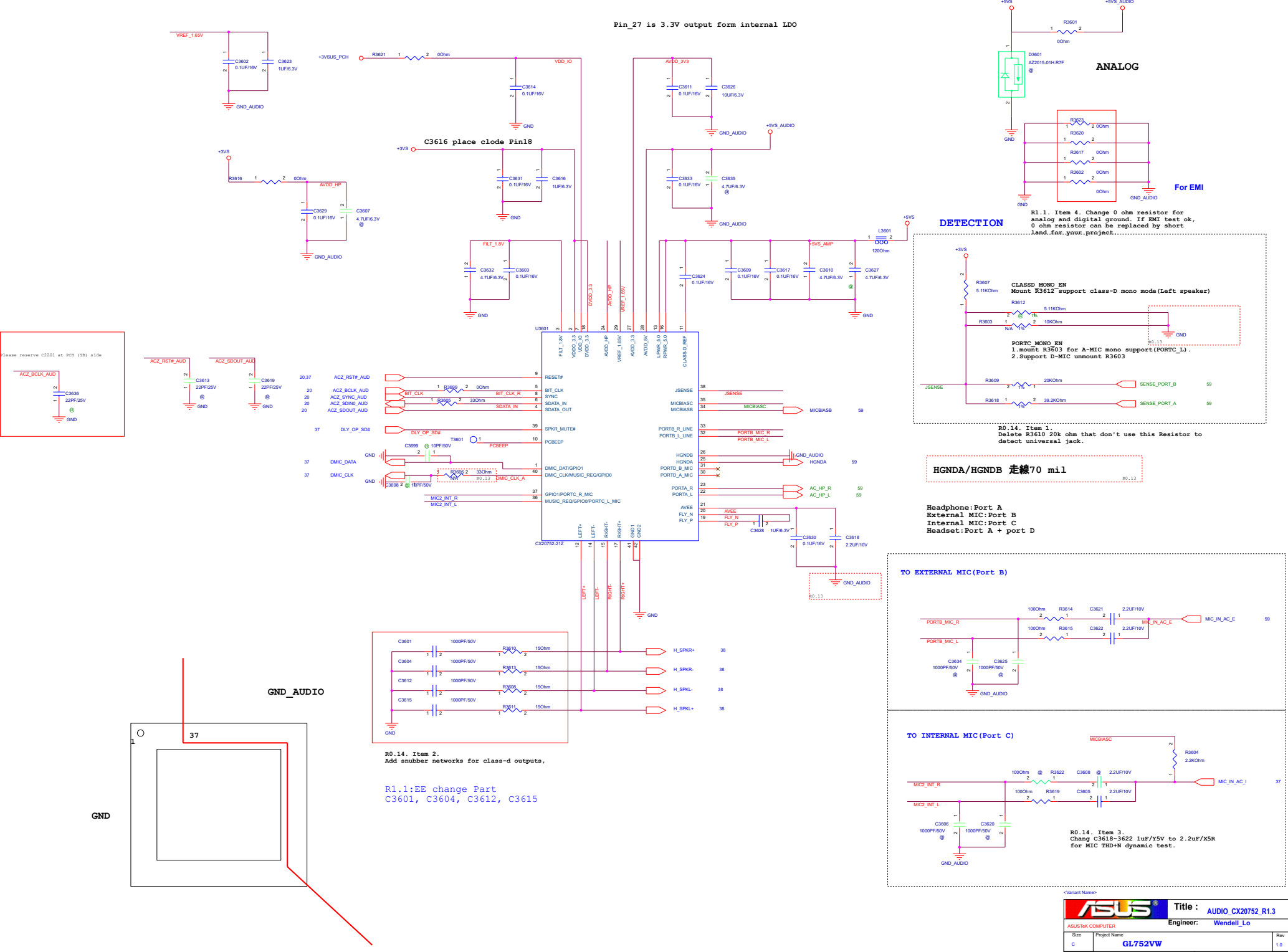
Title : LAN_*****

ASUSTeK COMPUTER

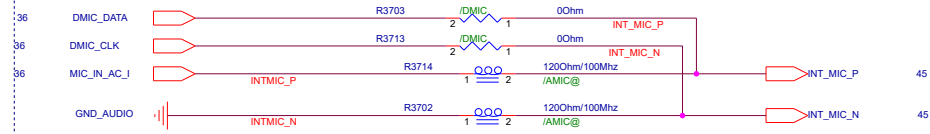
Engineer: Wendell_Lo

Size	Project Name	Rev
B	GL752VW	1.0

Pin_27 is 3.3V output form internal LDO

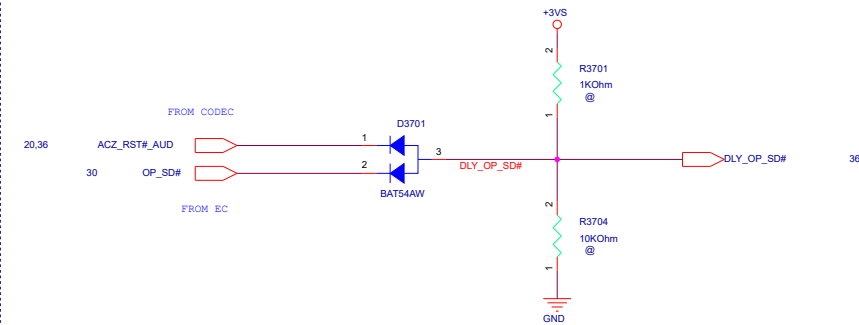


INTERNAL MICROPHONE



R2.0 change change R3714,R3702 from R to bead

MUTE CONTROL

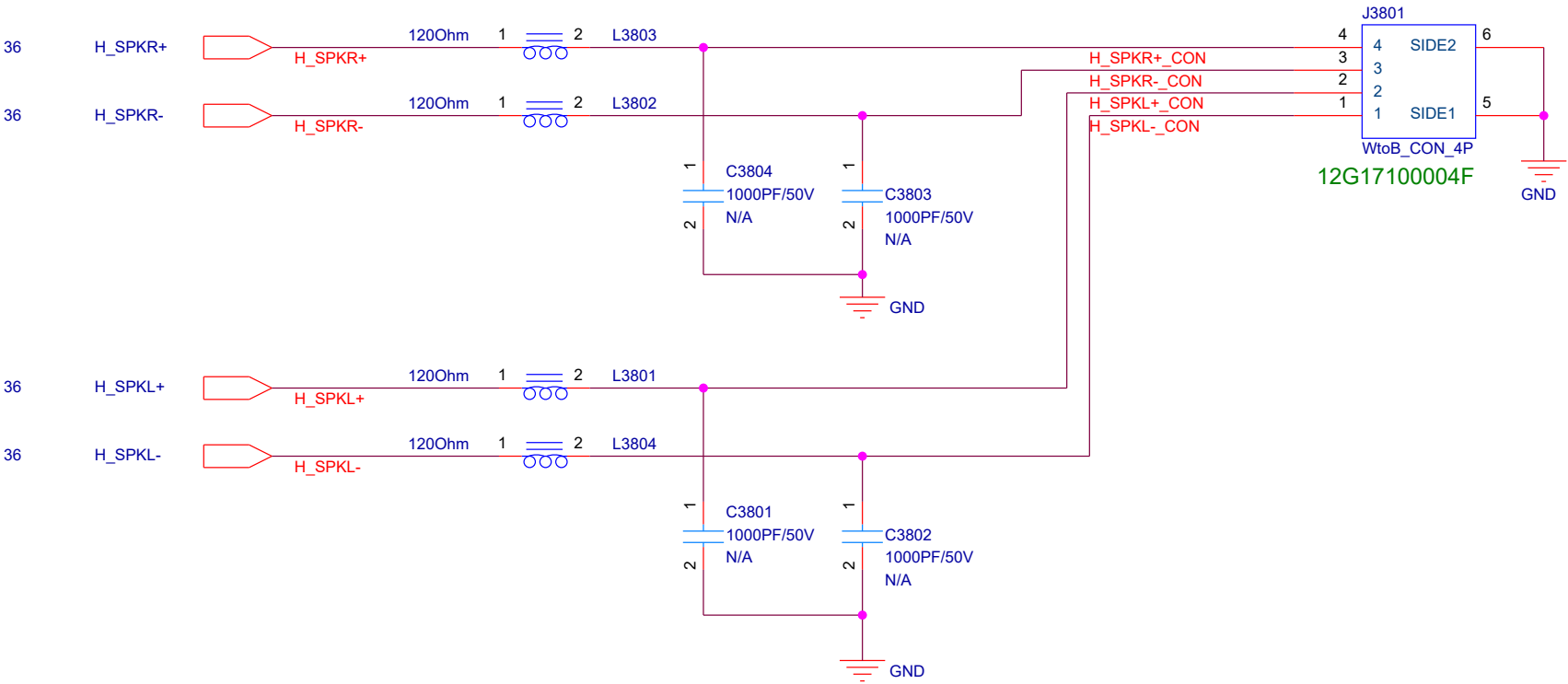


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<Variant Name>

		Title : AUD-AMP	
ASUSTek COMPUTER		Engineer: Wendell_Lo	
Size B	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 37 of 102	

PART NO	IMPEDANCE (Ω) AT100 MHz 500mV	DC RESISTANCE (Ω) Max	RATED CURRENT (mA) Max
ACMS160808A121 RDC05	120±25%	0.05	3000



<Variant Name>

		Title : AUD-MIC-IN__R1.4	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 38 of 102	



Title : **AUD_WOOFER**

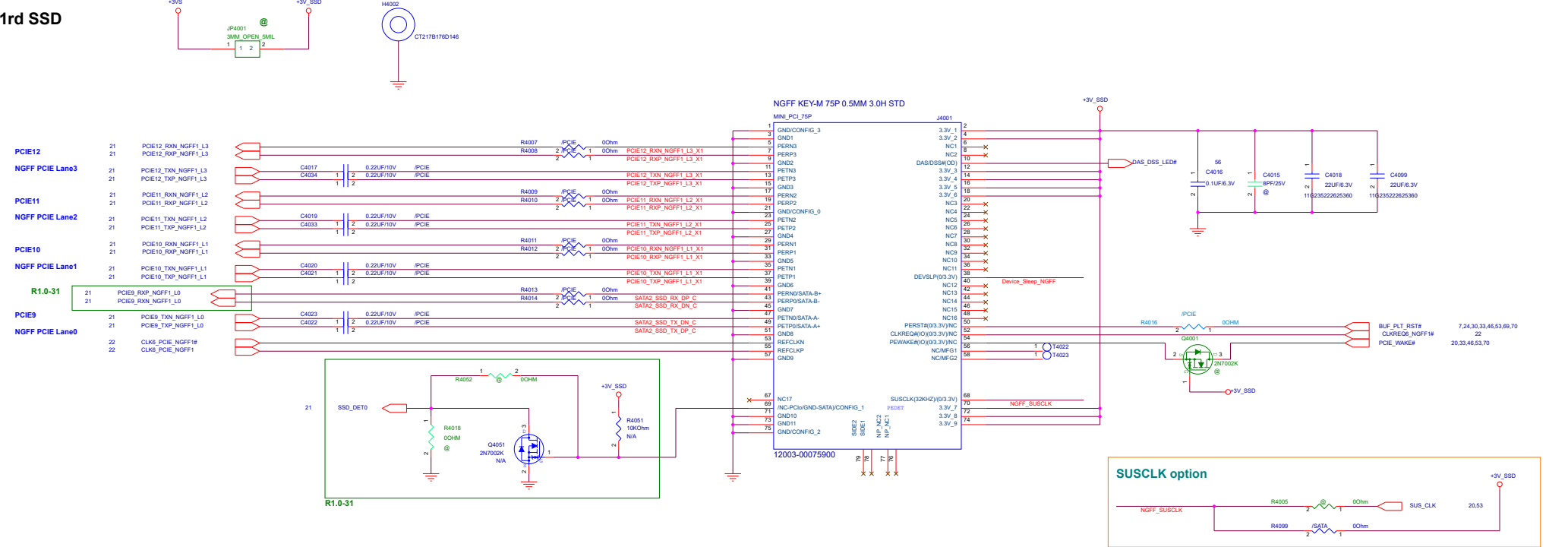
ASUSTeK COMPUTER

Engineer: **Wendell_Lo**

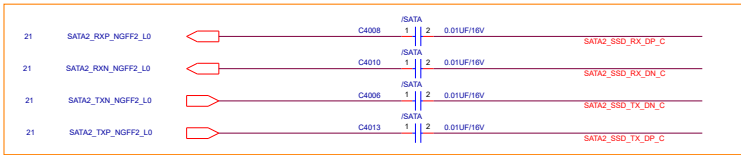
Size	Project Name
B	GL752VW

Rev
1.0

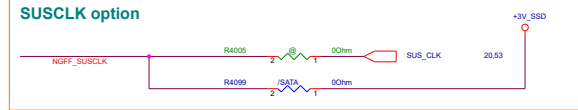
1rd SSD



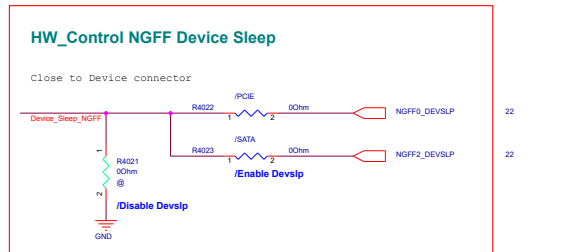
SATA SSD



SUSCLK option



R1.1-05 R0.1-43



HW Disable SSD Devslp	Mount R4021=0ohm, Unmount R4022 and R4023=0ohm
HW Enable SSD Devslp	Unmount R4021=0ohm, Mount R4022 or R4023=0ohm

<Variant Name>



Title : CLK_GEN

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name
B	GL752VW

Rev
1.0



Title : CB_RTS5139

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name
B	GL752VW

Rev
1.0



Project Name

GL752VW

Rev

1.0

Title : **DP to VGA_ANX6210**

Size

B

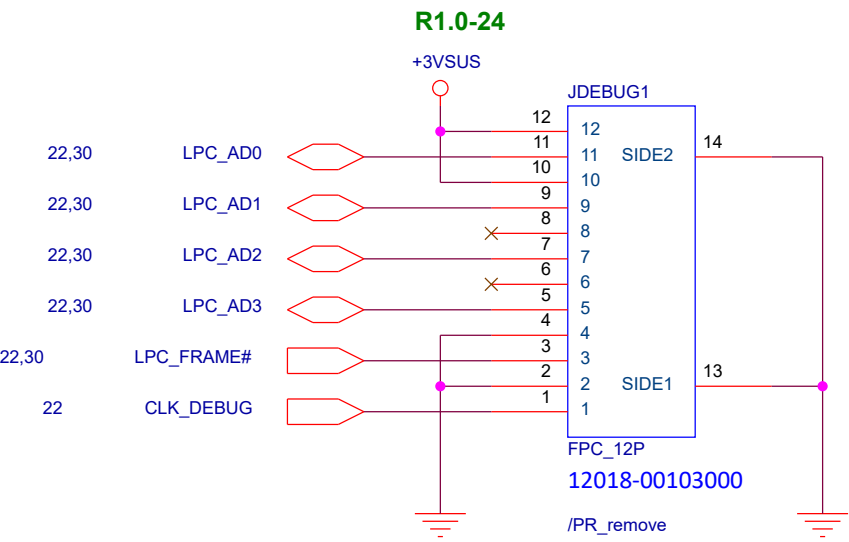
Dept.: **ASUSTeK COMPUTER**

Engineer: **Wendell_Lo**

Date: **Wednesday, September 23, 2015**

Sheet **43** of **102**

LPC Debug Port



		Title : DEBUG_LPC	
ASUSTeK COMPUTER		Engineer: Wendell_Lo	
Size A	Project Name GL752VW		Rev 1.0
Date: Wednesday, September 23, 2015		Sheet 44 of 102	

```
1k ohm resistor (0402) for 5% precise
: 10G212102004010

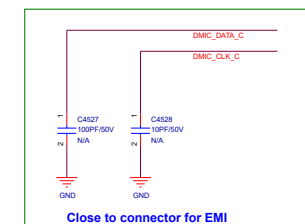
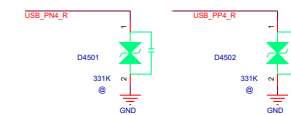
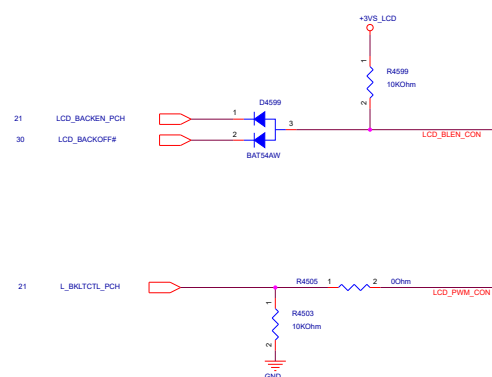
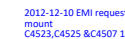
R4597 gives a current limitation for the PCM GP
when pin 3 is acted as flag# (103/05/13)
```

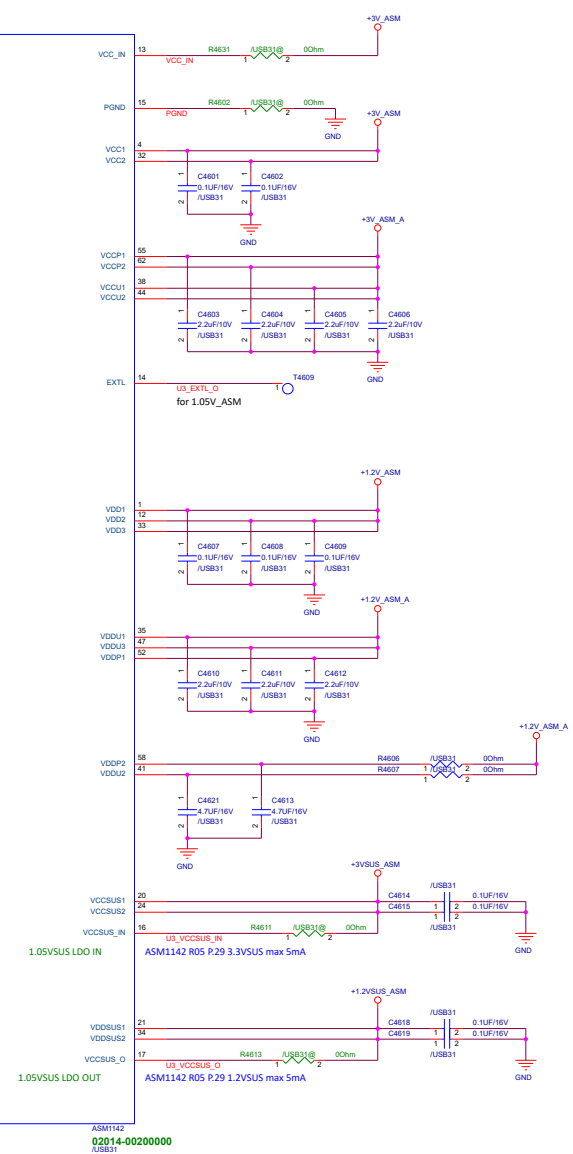
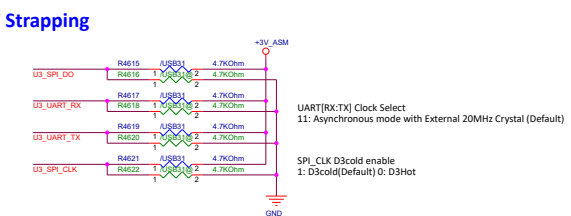
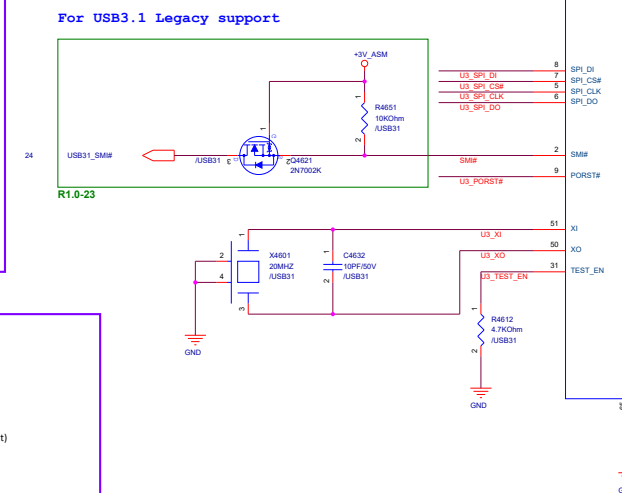
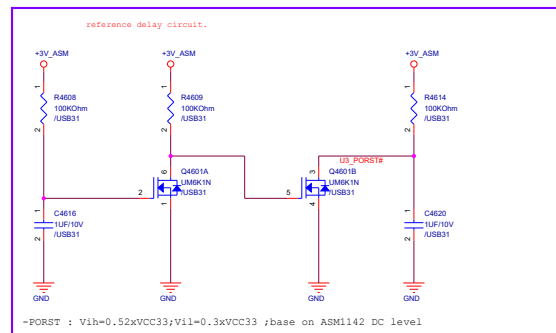
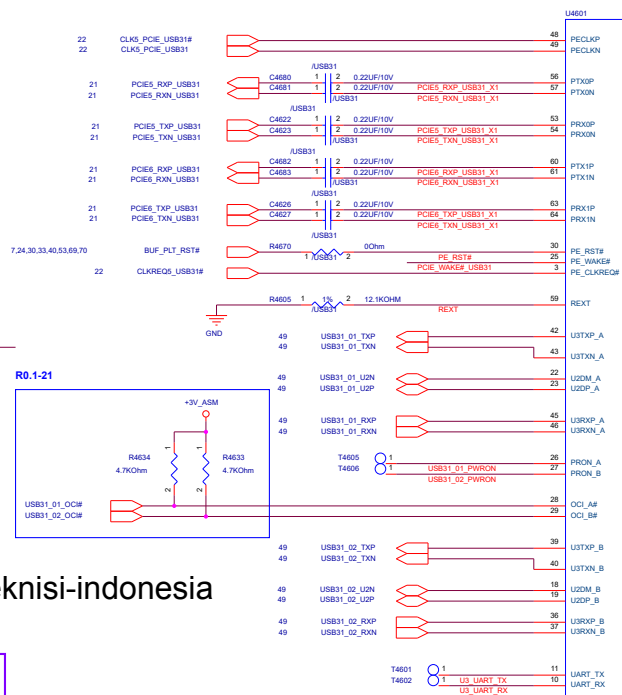
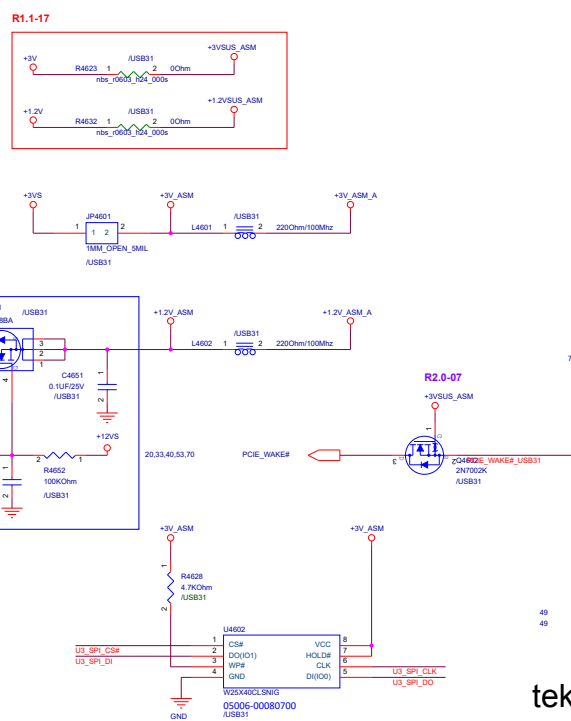


The schematic diagram illustrates the electrical connections for the EDP board. Key components and their values are as follows:

- Power Source:** A 3V5 voltage source is connected to a network of resistors and capacitors.
- Resistors:**
 - R4514: 100kOhm
 - R4516: 100kOhm
 - R4501: 100kOhm
 - R4504: 100kOhm
 - R4588: 3.0V
 - R4509: 100kOhm
- Capacitors:**
 - C4520: 0.1uF/6V
 - C4508: 0.1uF/6V
- Connections:**
 - The 3V5 source is connected to the EDP_TXND, EDP_TXPD, EDP_TXN1, and EDP_TXP1 modules.
 - The 3V5 source is also connected to the EDP_ALXP and EDP_ALXN modules.
 - The 3V5 source is connected to the EDP_TXND, EDP_TXPD, EDP_TXN1, and EDP_TXP1 modules.
 - The 3V5 source is connected to the EDP_ALXP and EDP_ALXN modules.
 - The 3V5 source is connected to the EDP_TXND, EDP_TXPD, EDP_TXN1, and EDP_TXP1 modules.
 - The 3V5 source is connected to the EDP_ALXP and EDP_ALXN modules.

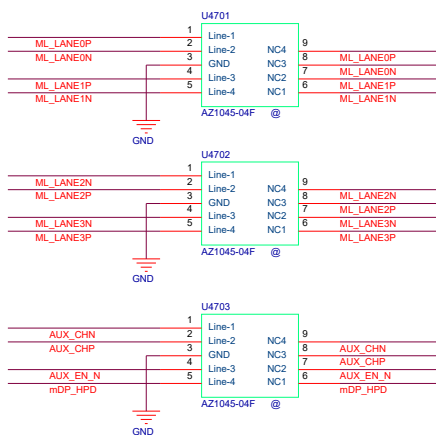
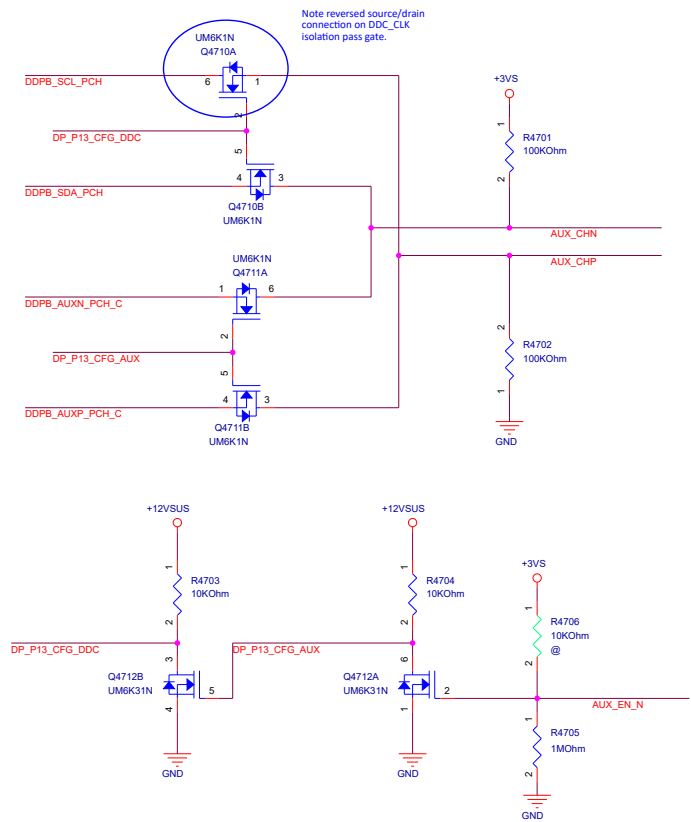
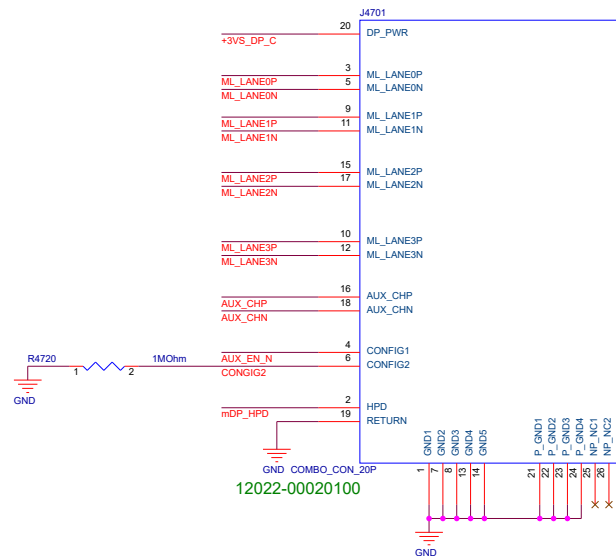
The schematic diagram illustrates the USB to RS-485 interface circuit. It features two USB ports, USB_PP4 and USB_PN4, connected to an RS-485 transceiver (RS485C2B) via L4501 ferrite beads. The transceiver is powered by a +3VS supply through a 120 Ohm resistor and a CAM_3V capacitor. The RS-485 output is connected to a C4501 capacitor and a 5.1UF18V capacitor, which are then connected to GND.

[illegible]



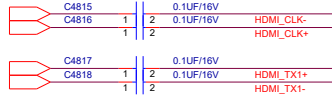
Main: 07013-00100000
2nd : 07013-00060200

The schematic diagram shows the R1.0-32 LED driver circuit. It features a +12V input connected to a 100kOhm resistor (R4708). The other end of R4708 is connected to the DP_HPD_L signal line. A 1MOhm resistor (R4721) is connected between DP_HPD_L and GND. The DP_HPD_L signal line also branches off to the mDP_HPD signal line. The mDP_HPD signal line is connected to the anode of the LED (Q4722 BSS138). The cathode of the LED is connected to GND. A 100kOhm resistor (R4728) is connected between the anode of the LED and GND. A 0.01uF25V capacitor (C4717) is connected between the anode of the LED and GND. The LED is labeled with its part number Q4722 BSS138 and its characteristics: $R_{ds(on)} = 5.8\Omega$ and $V_{gs(th)} = 1.6V$. The circuit is powered by GND.

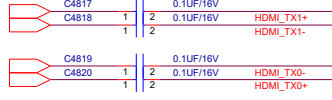


CPU DDIC

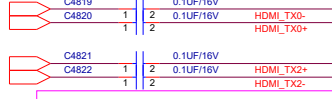
3 DDi2_TXN3_HDMI_CLK
3 DDi2_TXP3_HDMI_CLK



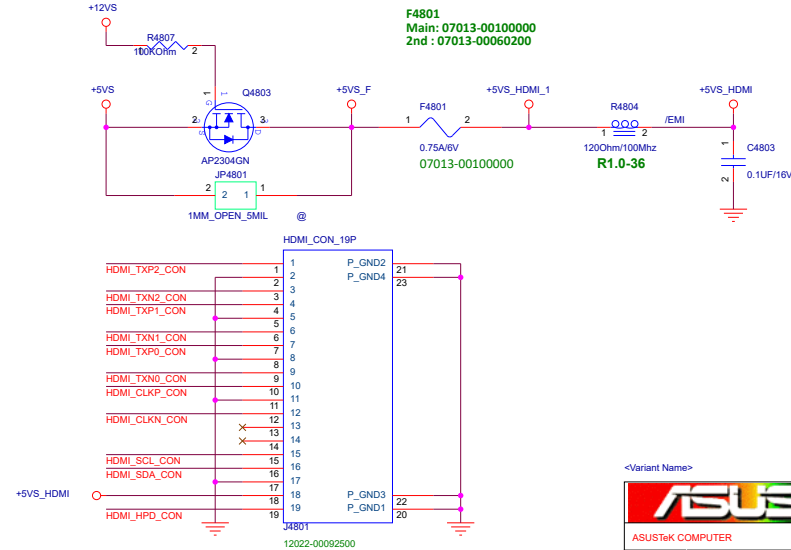
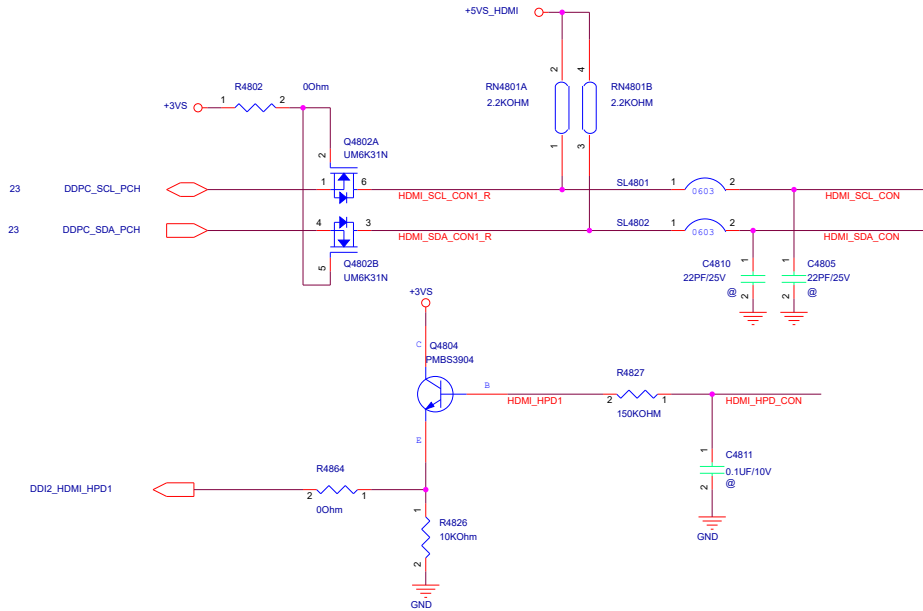
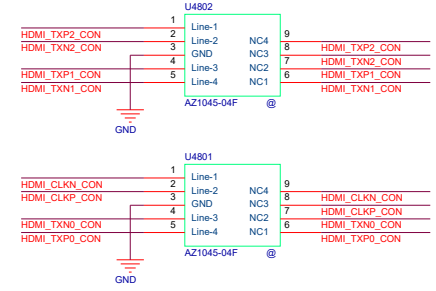
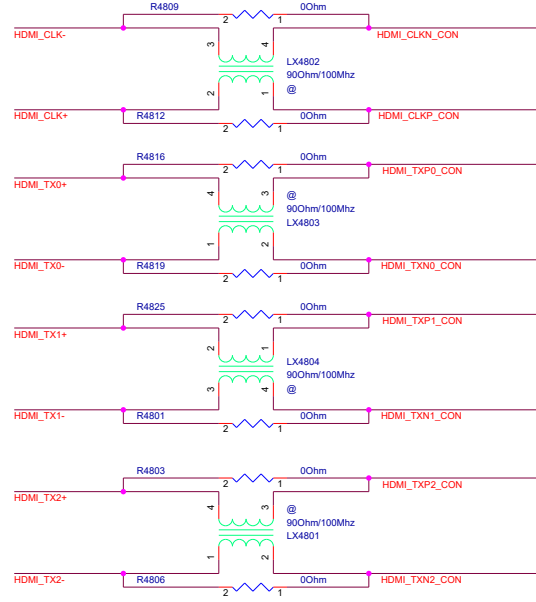
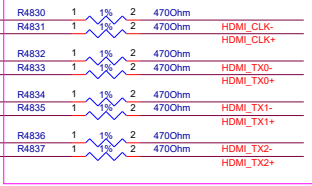
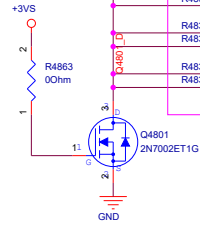
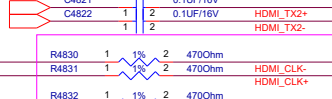
3 DDi2_TXP1_HDMI
3 DDi2_TXN1_HDMI



3 DDi2_TXN0_HDMI
3 DDi2_TXP0_HDMI



3 DDi2_TXP2_HDMI
3 DDi2_TXN2_HDMI



<Variant Name>

Figure 1: Schematic diagram of the proposed 100-Gb/s 4x4 optical switch. The diagram illustrates the internal structure of the switch, including input ports (21) labeled USB_P2 and USB_P1, and output ports (22) labeled USB_C_U2_N_X1, USB_C_U2_P_X1, USB_C_U3_N_X1, and USB_C_U3_P_X1. The switch is composed of two stages of 2x2 optical switches. The first stage uses two 2x2 optical switches (A1B2B1 and A2B2B1) and two 2x2 optical switches (A1B2B1 and A2B2B1). The second stage uses two 2x2 optical switches (A1B2B1 and A2B2B1) and two 2x2 optical switches (A1B2B1 and A2B2B1). The diagram also shows various components such as waveguides, couplers, and optical isolators.

Figure 10 shows two USB-C connector pinout diagrams. The left diagram is for a USB-C to USB-C connection, showing pins 1 through 24. The right diagram is for a USB-C to USB-A connection, showing pins 1 through 24. Both diagrams include labels for the pins and their corresponding signals.

Left Diagram (USB-C to USB-C):

- Pin 1:** D+ (USB_C_USB_X1)
- Pin 2:** D- (USB_C_USB_X1)
- Pin 3:** VBUS (USB_C_USB_VAN_X1)
- Pin 4:** NC1 (USB_C_USB_VAN_X1)
- Pin 5:** TX+ (USB_C_USB_VAN_X1)
- Pin 6:** TX- (USB_C_USB_VAN_X1)
- Pin 7:** RX+ (USB_C_USB_VAN_X1)
- Pin 8:** RX- (USB_C_USB_VAN_X1)
- Pin 9:** GND
- Pin 10:** GND
- Pin 11:** D+ (USB_C_USB_F_X1)
- Pin 12:** D- (USB_C_USB_F_X1)
- Pin 13:** VBUS (USB_C_USB_F_X1)
- Pin 14:** NC2 (USB_C_USB_F_X1)
- Pin 15:** TX+ (USB_C_USB_F_X1)
- Pin 16:** TX- (USB_C_USB_F_X1)
- Pin 17:** RX+ (USB_C_USB_F_X1)
- Pin 18:** RX- (USB_C_USB_F_X1)
- Pin 19:** GND
- Pin 20:** GND
- Pin 21:** GND
- Pin 22:** GND
- Pin 23:** GND
- Pin 24:** GND

Right Diagram (USB-C to USB-A):

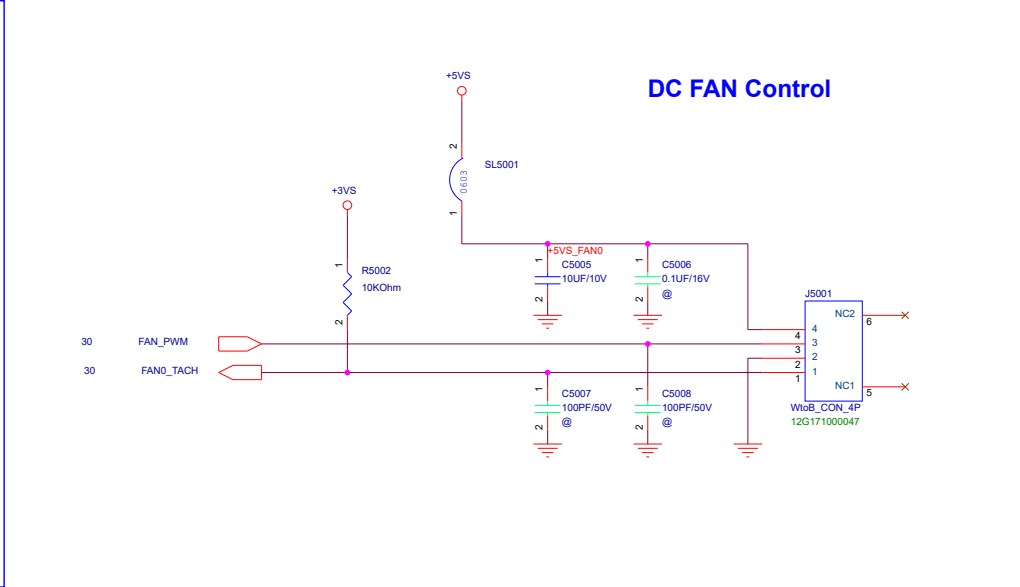
- Pin 1:** D+ (USB_C_USB_X1)
- Pin 2:** D- (USB_C_USB_X1)
- Pin 3:** VBUS (USB_C_USB_VAN_X1)
- Pin 4:** NC1 (USB_C_USB_VAN_X1)
- Pin 5:** TX+ (USB_C_USB_VAN_X1)
- Pin 6:** TX- (USB_C_USB_VAN_X1)
- Pin 7:** RX+ (USB_C_USB_VAN_X1)
- Pin 8:** RX- (USB_C_USB_VAN_X1)
- Pin 9:** GND
- Pin 10:** GND
- Pin 11:** D+ (USB_C_USB_F_X1)
- Pin 12:** D- (USB_C_USB_F_X1)
- Pin 13:** VBUS (USB_C_USB_F_X1)
- Pin 14:** NC2 (USB_C_USB_F_X1)
- Pin 15:** TX+ (USB_C_USB_F_X1)
- Pin 16:** TX- (USB_C_USB_F_X1)
- Pin 17:** RX+ (USB_C_USB_F_X1)
- Pin 18:** RX- (USB_C_USB_F_X1)
- Pin 19:** GND
- Pin 20:** GND
- Pin 21:** GND
- Pin 22:** GND
- Pin 23:** GND
- Pin 24:** GND

[illegible]

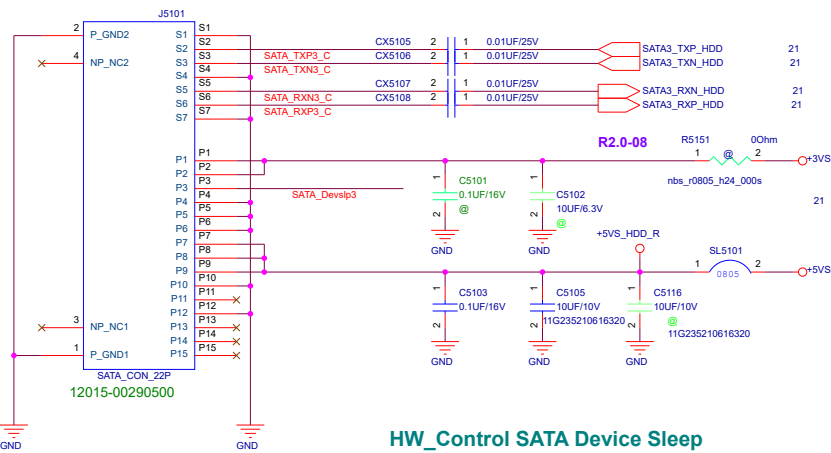
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The schematic diagram illustrates the USB-to-UART bridge circuit for the ESP8266 module. Key components and connections include:

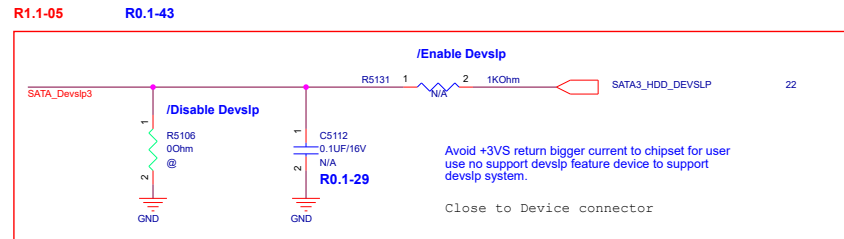
- USB-to-UART Bridge IC (U4805):** This IC is connected to the USB side via pins 1 (D+), 2 (D-), 3 (NC), 4 (GND), 5 (VCC), 6 (NC), 7 (NC), 8 (NC), 9 (NC), 10 (NC), 11 (NC), 12 (NC), 13 (VCC), 14 (GND), 15 (GND), 16 (GND), 17 (GND), 18 (GND), 19 (GND), 20 (GND), 21 (GND), 22 (GND), 23 (GND), 24 (GND), 25 (GND), 26 (GND), 27 (GND), 28 (GND), 29 (GND), 30 (GND), 31 (GND), 32 (GND), 33 (GND), 34 (GND), 35 (GND), 36 (GND), 37 (GND), 38 (GND), 39 (GND), 40 (GND), 41 (GND), 42 (GND), 43 (GND), 44 (GND), 45 (GND), 46 (GND), 47 (GND), 48 (GND), 49 (GND), 50 (GND), 51 (GND), 52 (GND), 53 (GND), 54 (GND), 55 (GND), 56 (GND), 57 (GND), 58 (GND), 59 (GND), 60 (GND), 61 (GND), 62 (GND), 63 (GND), 64 (GND), 65 (GND), 66 (GND), 67 (GND), 68 (GND), 69 (GND), 70 (GND), 71 (GND), 72 (GND), 73 (GND), 74 (GND), 75 (GND), 76 (GND), 77 (GND), 78 (GND), 79 (GND), 80 (GND), 81 (GND), 82 (GND), 83 (GND), 84 (GND), 85 (GND), 86 (GND), 87 (GND), 88 (GND), 89 (GND), 90 (GND), 91 (GND), 92 (GND), 93 (GND), 94 (GND), 95 (GND), 96 (GND), 97 (GND), 98 (GND), 99 (GND), 100 (GND).
- USB-to-UART Bridge IC (U4801):** This IC is connected to the UART side via pins 1 (D+), 2 (D-), 3 (NC), 4 (GND), 5 (VCC), 6 (NC), 7 (NC), 8 (NC), 9 (NC), 10 (NC), 11 (NC), 12 (NC), 13 (VCC), 14 (GND), 15 (GND), 16 (GND), 17 (GND), 18 (GND), 19 (GND), 20 (GND), 21 (GND), 22 (GND), 23 (GND), 24 (GND), 25 (GND), 26 (GND), 27 (GND), 28 (GND), 29 (GND), 30 (GND), 31 (GND), 32 (GND), 33 (GND), 34 (GND), 35 (GND), 36 (GND), 37 (GND), 38 (GND), 39 (GND), 40 (GND), 41 (GND), 42 (GND), 43 (GND), 44 (GND), 45 (GND), 46 (GND), 47 (GND), 48 (GND), 49 (GND), 50 (GND), 51 (GND), 52 (GND), 53 (GND), 54 (GND), 55 (GND), 56 (GND), 57 (GND), 58 (GND), 59 (GND), 60 (GND), 61 (GND), 62 (GND), 63 (GND), 64 (GND), 65 (GND), 66 (GND), 67 (GND), 68 (GND), 69 (GND), 70 (GND), 71 (GND), 72 (GND), 73 (GND), 74 (GND), 75 (GND), 76 (GND), 77 (GND), 78 (GND), 79 (GND), 80 (GND), 81 (GND), 82 (GND), 83 (GND), 84 (GND), 85 (GND), 86 (GND), 87 (GND), 88 (GND), 89 (GND), 90 (GND), 91 (GND), 92 (GND), 93 (GND), 94 (GND), 95 (GND), 96 (GND), 97 (GND), 98 (GND), 99 (GND), 100 (GND).
- Passive Components:** The circuit includes various resistors (R4907, R4908, R4909, R4910, R4911, R4912, R4913, R4914, R4915, R4916, R4917, R4918, R4919, R4920, R4921, R4922, R4923, R4924, R4925, R4926, R4927, R4928, R4929, R4930, R4931, R4932, R4933, R4934, R4935, R4936, R4937, R4938, R4939, R4940, R4941, R4942, R4943, R4944, R4945, R4946, R4947, R4948, R4949, R4950, R4951, R4952, R4953, R4954, R4955, R4956, R4957, R4958, R4959, R4960, R4961, R4962, R4963, R4964, R4965, R4966, R4967, R4968, R4969, R4970, R4971, R4972, R4973, R4974, R4975, R4976, R4977, R4978, R4979, R4980, R4981, R4982, R4983, R4984, R4985, R4986, R4987, R4988, R4989, R4990, R4991, R4992, R4993, R4994, R4995, R4996, R4997, R4998, R4999, R5000, R5001, R5002, R5003, R5004, R5005, R5006, R5007, R5008, R5009, R5010, R5011, R5012, R5013, R5014, R5015, R5016, R5017, R5018, R5019, R5020, R5021, R5022, R5023, R5024, R5025, R5026, R5027, R5028, R5029, R5030, R5031, R5032, R5033, R5034, R5035, R5036, R5037, R5038, R5039, R5040, R5041, R5042, R5043, R5044, R5045, R5046, R5047, R5048, R5049, R5050, R5051, R5052, R5053, R5054, R5055, R5056, R5057, R5058, R5059, R5060, R5061, R5062, R5063, R5064, R5065, R5066, R5067, R5068, R5069, R5070, R5071, R5072, R5073, R5074, R5075, R5076, R5077, R5078, R5079, R5080, R5081, R5082, R5083, R5084, R5085, R5086, R5087, R5088, R5089, R5090, R5091, R5092, R5093, R5094, R5095, R5096, R5097, R5098, R5099, R5100, R5101, R5102, R5103, R5104, R5105, R5106, R5107, R5108, R5109, R5110, R5111, R5112, R5113, R5114, R5115, R5116, R5117, R5118, R5119, R5120, R5121, R5122, R5123, R5124, R5125, R5126, R5127, R5128, R5129, R5130, R5131, R5132, R5133, R5134, R5135, R5136, R5137, R5138, R5139, R5140, R5141, R5142, R5143, R5144, R5145, R5146, R5147, R5148, R5149, R5150, R5151, R5152, R5153, R5154, R5155, R5156, R5157, R5158, R5159, R5160, R5161, R5162, R5163, R5164, R5165, R5166, R5167, R5168, R5169, R5170, R5171, R5172, R5173, R5174, R5175, R5176, R5177, R5178, R5179, R5180, R5181, R5182, R5183, R5184, R5185, R5186, R5187, R5188, R5189, R5190, R5191, R5192, R5193, R5194, R5195, R5196, R5197, R5198, R5199, R5200, R5201, R5202, R5203, R5204, R5205, R5206, R5207, R5208, R5209, R5210, R5211, R5212, R5213, R5214, R5215, R5216, R5217, R5218, R5219, R5220, R5221, R5222, R5223, R5224, R5225, R5226, R5227, R5228, R5229, R5230, R5231, R5232, R5233, R5234, R5235, R5236, R5237, R5238, R5239, R5240, R5241, R5242, R5243, R5244, R5245, R5246, R5247, R5248, R5249, R5250, R5251, R5252, R5253, R5254, R5255, R5256, R5257, R5258, R5259, R5260, R5261, R5262, R5263, R5264, R5265, R5266, R5267, R5268, R5269, R5270, R5271, R5272, R5273, R5274, R5275, R5276, R5277, R5278, R5279, R5280, R5281, R5282, R5283, R5284, R5285, R5286, R5287, R5288, R5289, R5290, R5291, R5292, R5293, R5294, R5295, R5296, R5297, R5298, R5299, R5300, R5301, R5302, R5303, R5304, R5305, R5306, R5307, R5308, R5309, R5310, R5311, R5312, R5313, R5314, R5315, R5316, R5317, R5318, R5319, R5320, R5321, R5322,

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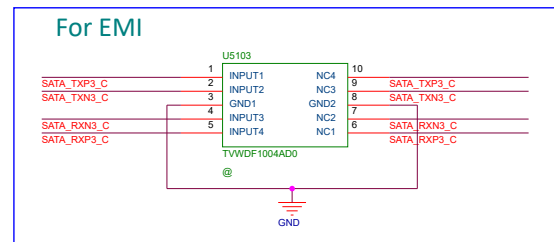
Main HDD



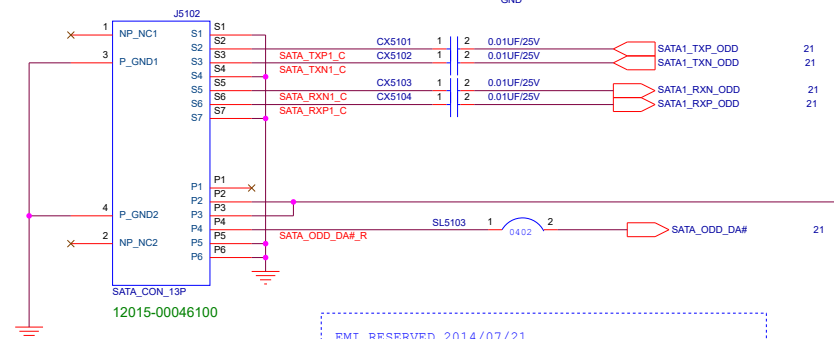
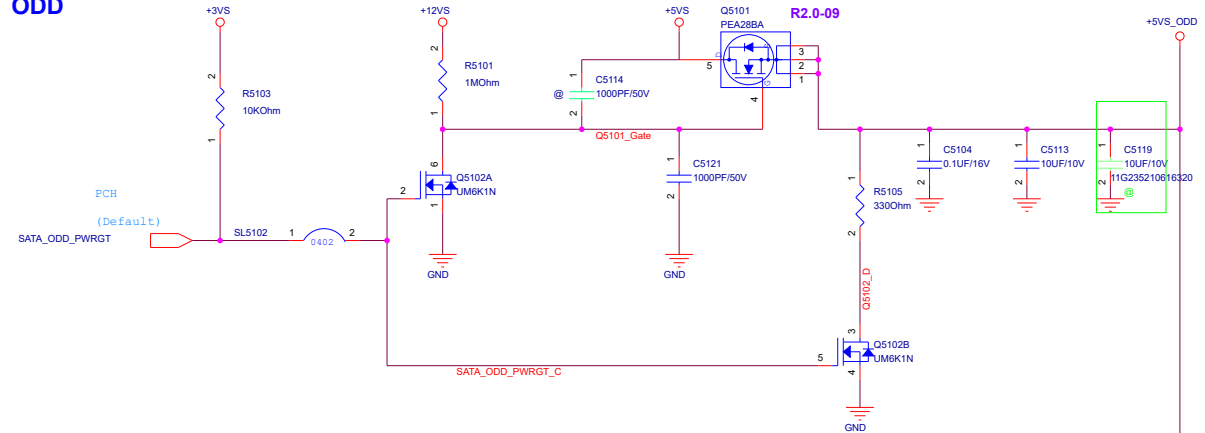
HW_Control SATA Device Sleep



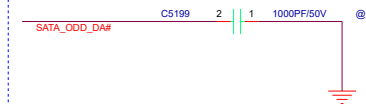
For EMI



ODD



EMI RESERVED 2014/07/21

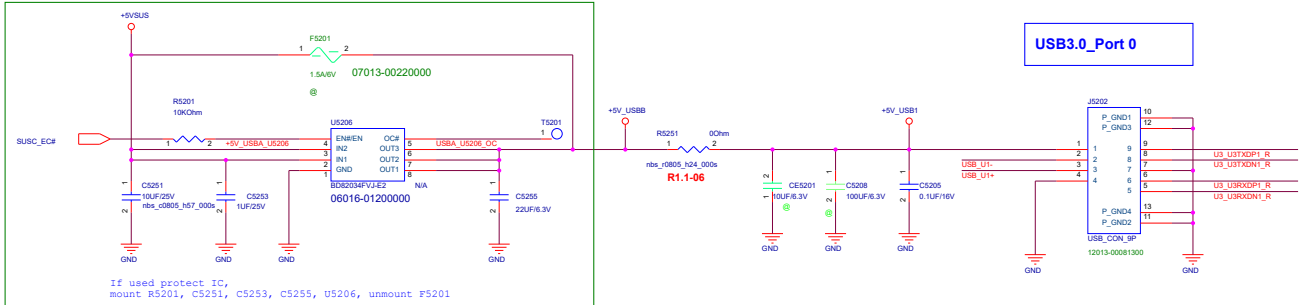
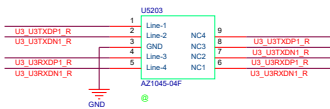
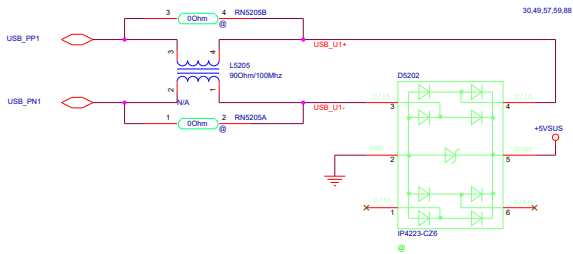


EMI-Protection

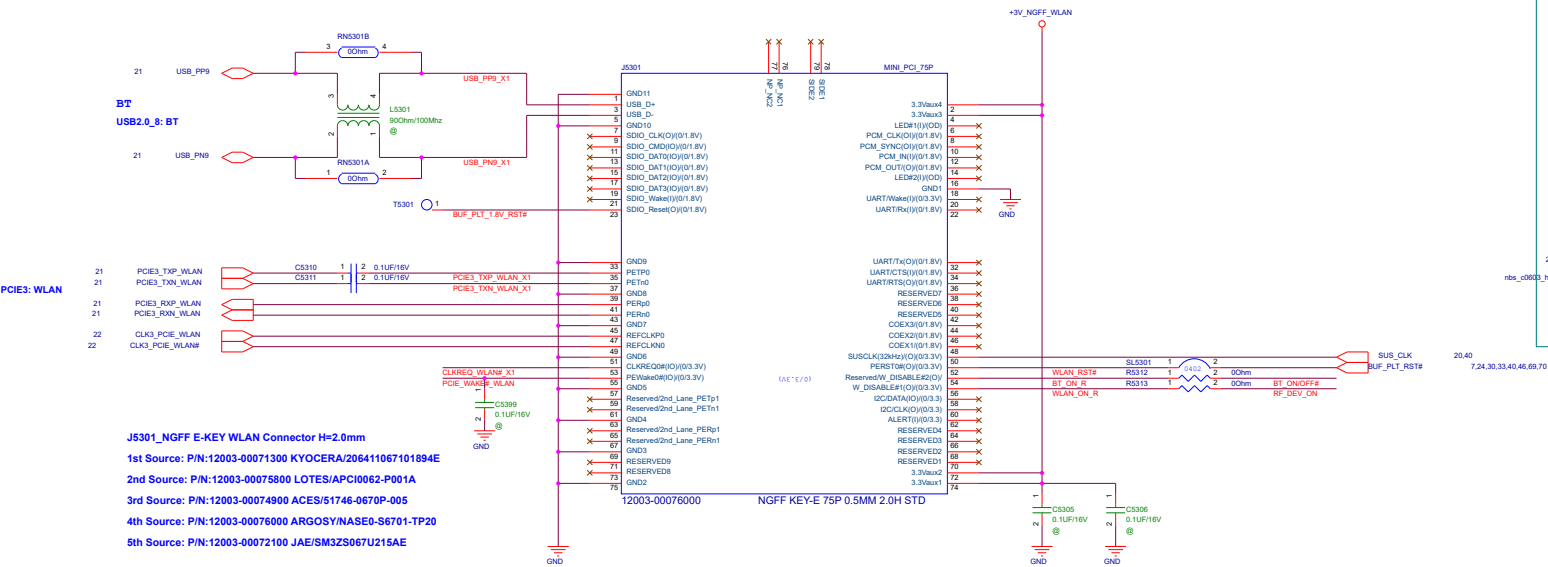
12/10/25
L5201, L5202, L5203, L5204
09G092090400



USB2.0 EMI-Protection

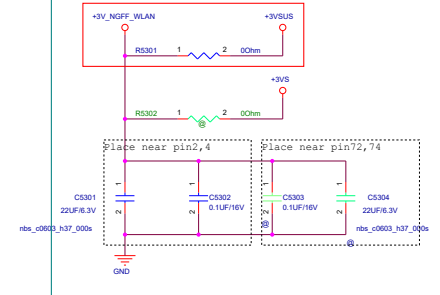


NGFF M.2 TYPE_E-KEY WIFI

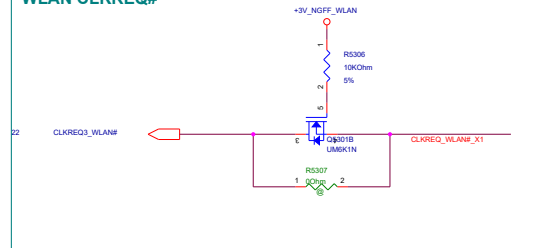


WLAN PWR_+3V_NGFF_WLAN (Non-ISCT)

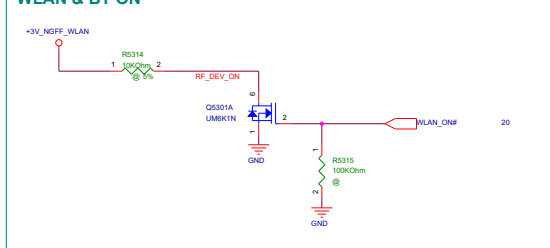
Support ASUS Open Cloud Computing (AOConnect)
WLAN PWR to +3VSUS



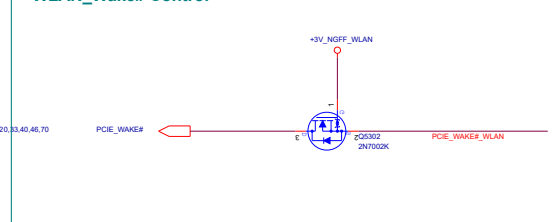
WLAN CLKREQ#



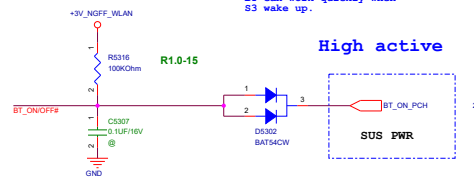
WLAN & BT ON



WLAN_Wake# Control

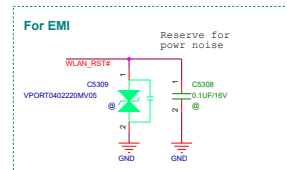


To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.



Project which use the combo card schematic should make sure that BT_ON signal can't be High at S3/S4/S5 state to prevent leakage

For EMI



74	1.3Vaux	GN0	75
72	3.3Vaux	RESERVED	73
70	RESERVED	RESERVED	71
68	RESERVED	GN0	69
66	RESERVED	Reserved/2nd Lane PETn1	67
64	GPIO NFC Reset# (MCP107)(O/0.3V)	Reserved/2nd Lane PETp1	65
62	NFC DC IRQ (MCP05)(I/O/3.3)	GN0	63
60	NFC DC SM CLK_0 (I/O/3.3)	Reserved/2nd Lane PETn1	61
58	NFC DC SM CLK_1 (I/O/3.3)	Reserved/2nd Lane PETp1	59
56	W_DISABLE1 (O/0.3V)	GN0	57
54	Reserved/W_DISABLE2 (O/0.3V)	PEWAKE0 (O/0.3V)	55
52	PET0T0 (O/0.3V)	CLKREQ0 (IO/0.3V)	53
50	SUSCLK(32KHz) (O/0.3V)	GN0	51
48	CODK1(7/0.18V)	REFCLKN0	49
46	CODK2(7/0.18V)	REFCLKP0	47
44	CODK3(7/0.18V)	PETn0	45
42	Clrk CLK	PETp0	43
40	Clrk DATA	GN0	41
38	Clrk RESET (O/0.3V)	GN0	39
36	UART CT5 (O/0.18V)	PETn0	37
34	UART RT5 (I/O/0.18V)	PETp0	35
32	UART Tx (O/0.18V)	GN0	33
	Key	Key	
	Key	Key	
	Key	Key	
	Key	Key	
22	UART Rx (I/O/0.18V)	SDIO Reset(O/0.3V)	23
20	UART Wake (I/0.3V)	SDIO Wake(I/O/0.3V)	21
18	GN0	SDIO DAT3(O/0.3V)	19
16	LED0 (HOD)	SDIO DAT2(O/0.3V)	17
14	PCM_OUT (I/O/0.18V)	SDIO DAT1(O/0.3V)	15
12	PCM_IN (O/0.18V)	SDIO DATA(O/0.3V)	13
10	PCM_SYNC (O/0.18V)	SDIO CMD(O/0.3V)	11
8	PCM_CLK (O/0.18V)	SDIO CLK(D/0.3V)	9
6	LEDW1 (HOD)	GN0	7
4	1.3Vaux	USB_D-	5
2	1.3Vaux	USB_D+	3
		GN0	1

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Title : USB3_*****

ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name
B	GL752VW

Rev
1.0



Title : USB3_*****

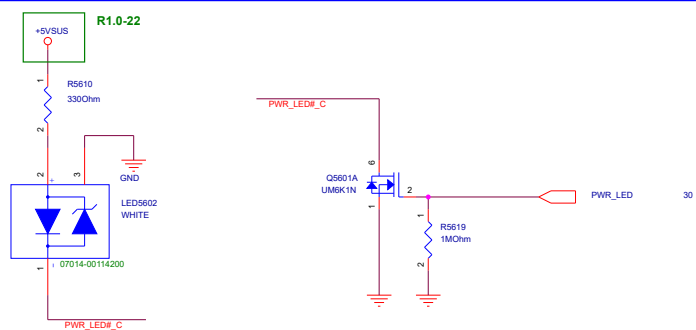
ASUSTeK COMPUTER

Engineer: Wendell_Lo

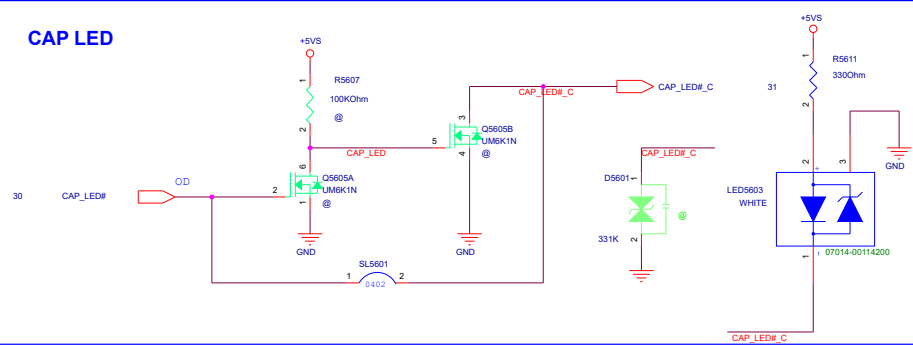
Size	Project Name
B	GL752VW

Rev
1.0

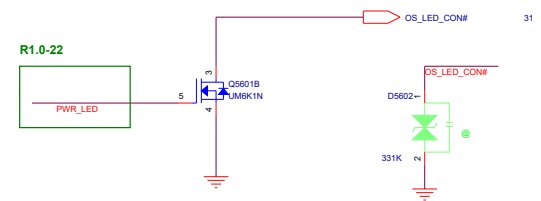
POWER LED



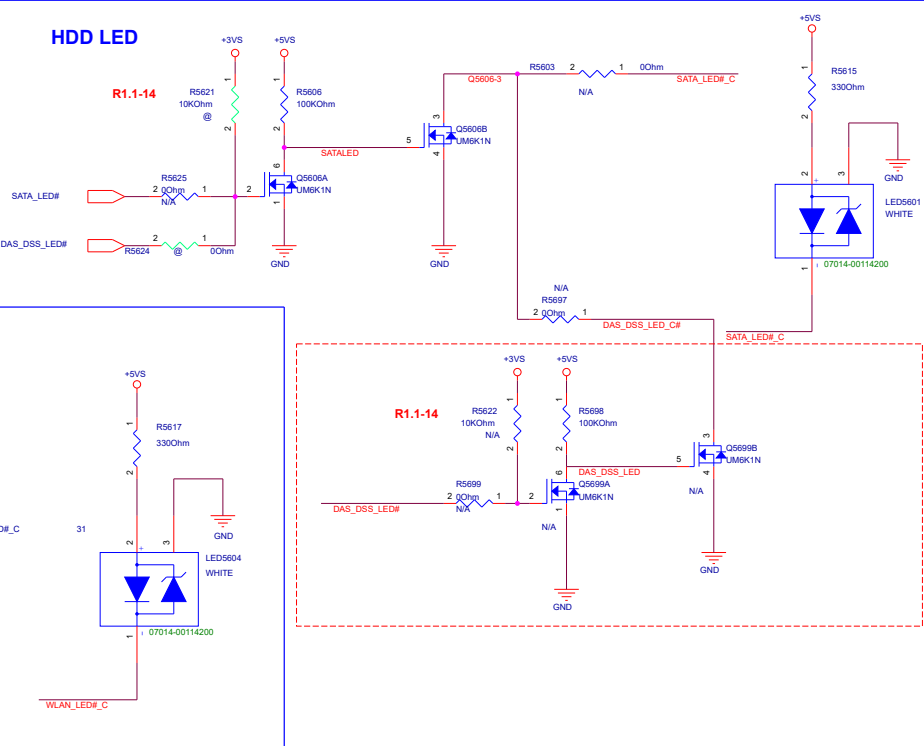
CAP LED



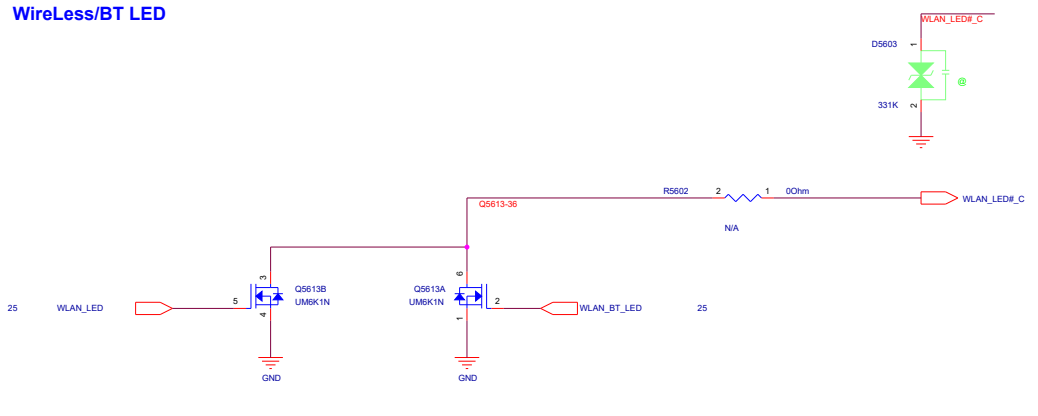
OS_LED#



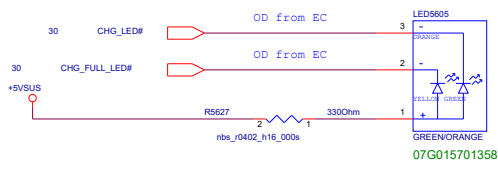
HDD LED



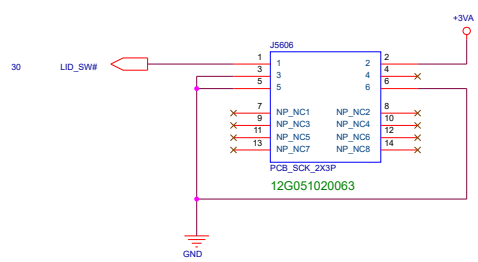
WireLess/BT LED



Charger LED



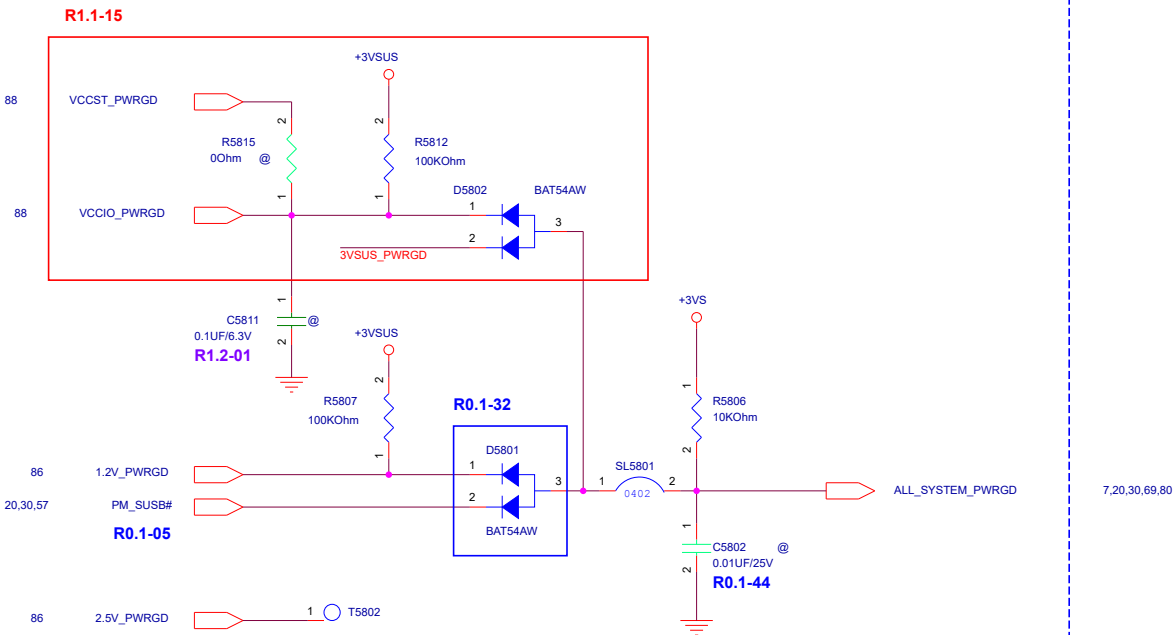
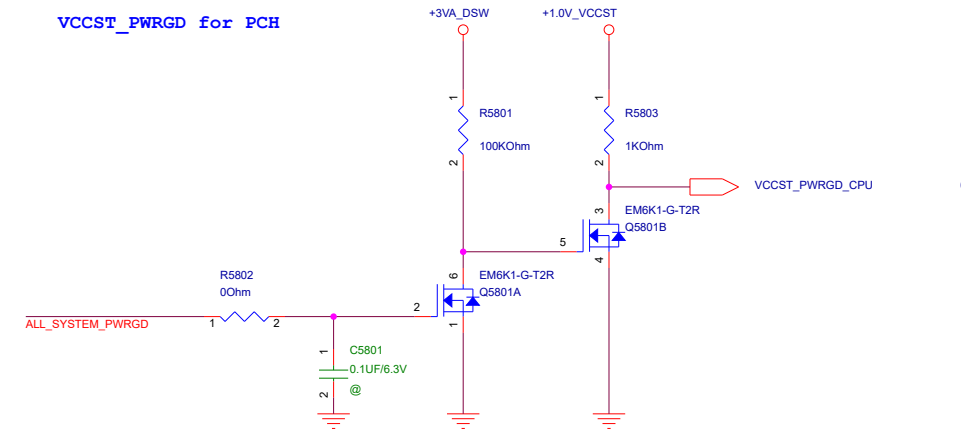
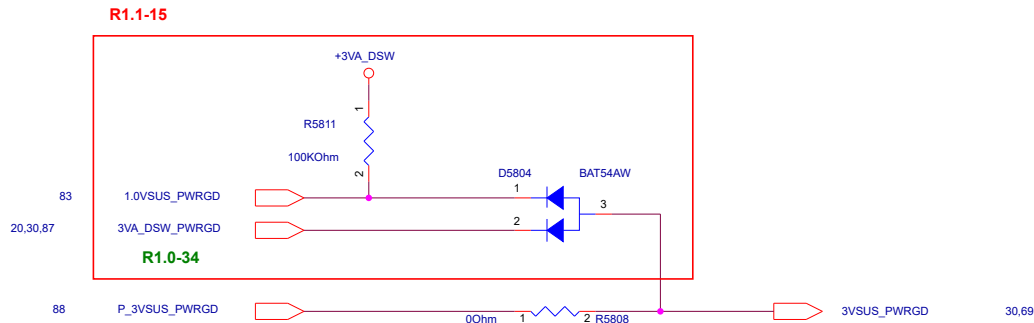
LID SW @ LID board





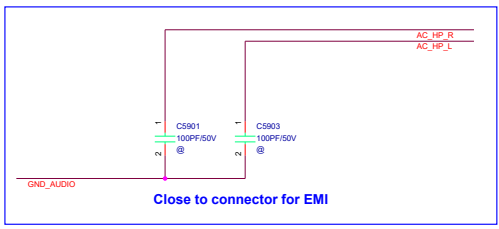
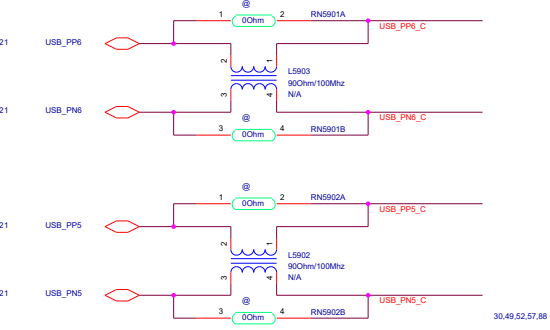
每小時耗 0.45mW
每個月耗 324mW
 $0.45\text{mW} = (15 \times 15 / 1\text{M}) \times 2$



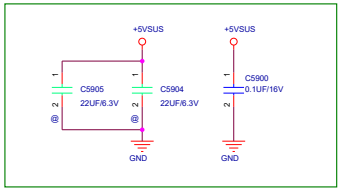


<Variant Name>

ASUS		Title : Power Protect	
ASUSTek COMPUTER		Engineer: Wendell_Lo	
Size	Project Name	GL752VW	Rev
Custom			1.0
Date:	Wednesday, September 23, 2015	Sheet	58 of 102



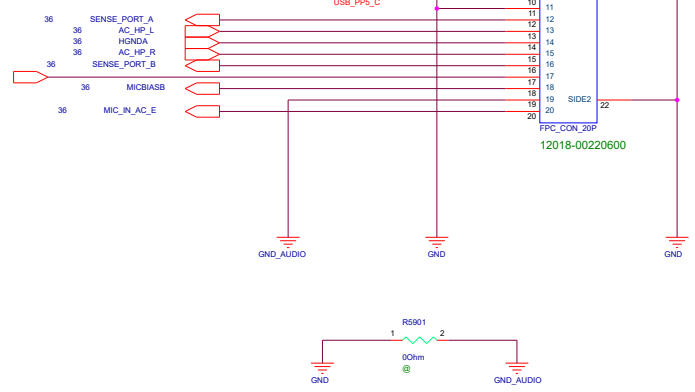
R1.0-28



To I/O Board

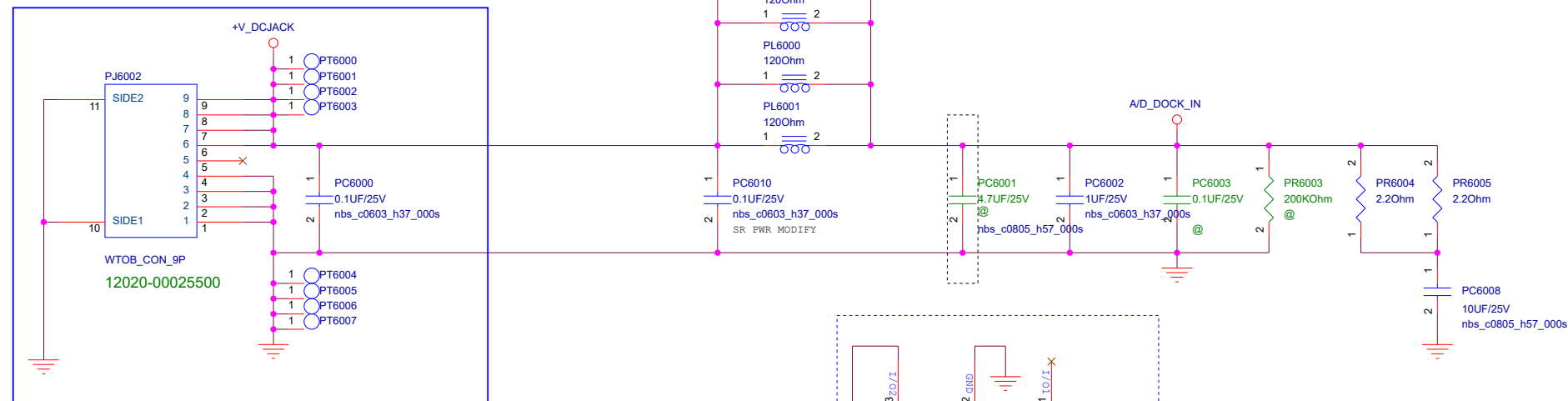
R1.0-28

SUSC_EC#

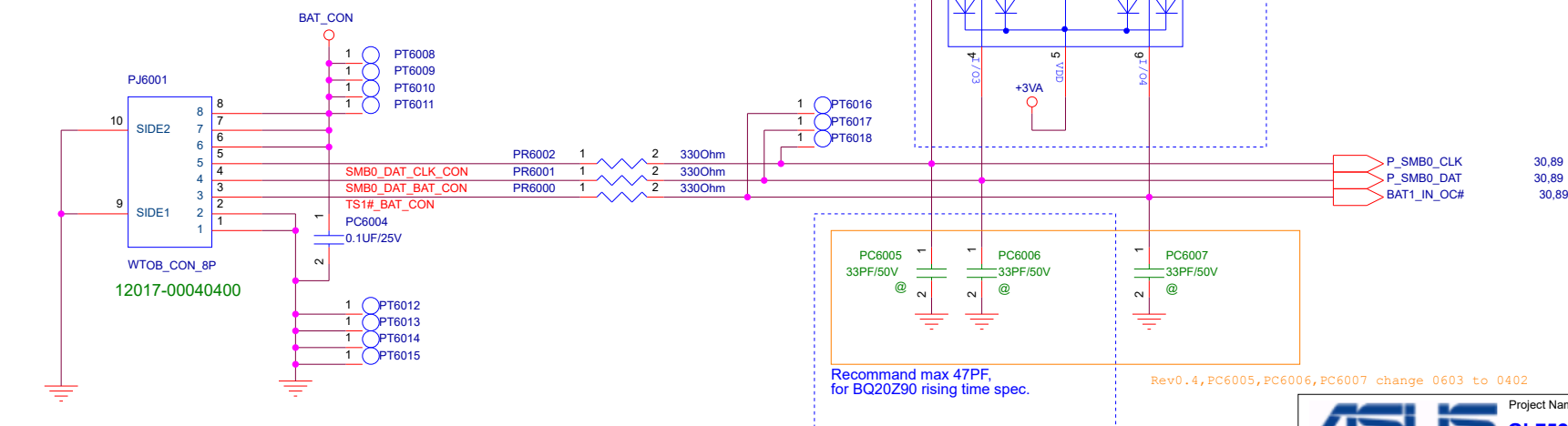


DC-IN Connector

R0.1-15

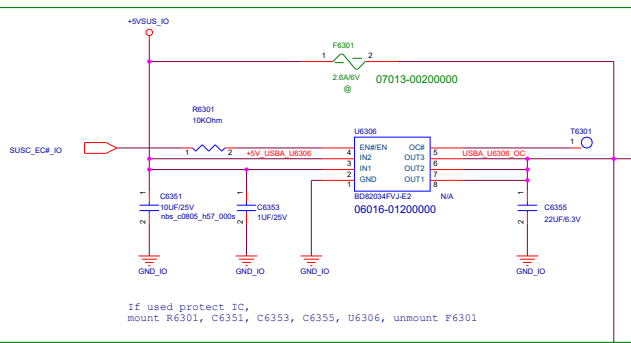


Battery Connector

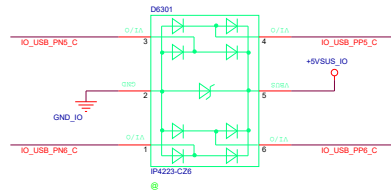
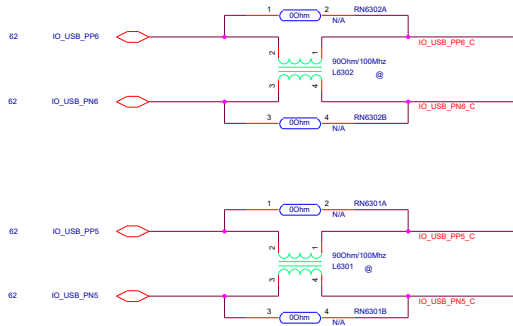
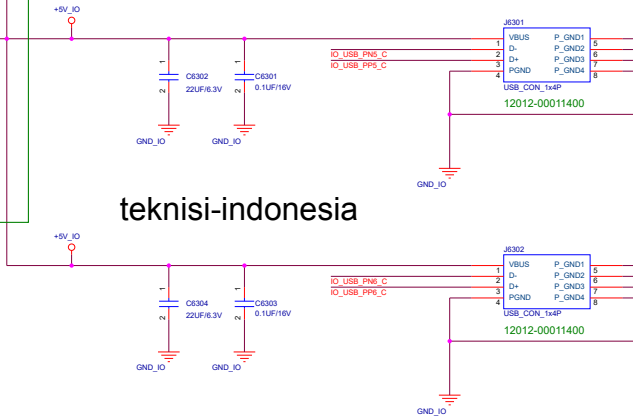


081111 -> 090604:
1. Change PD6005 from DF5A6.8FU to IP4223-CZ6 for cost down and integration.

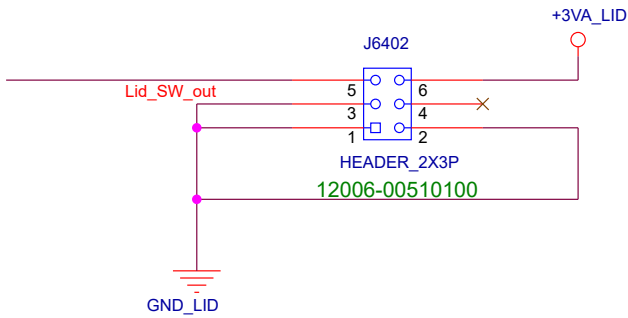
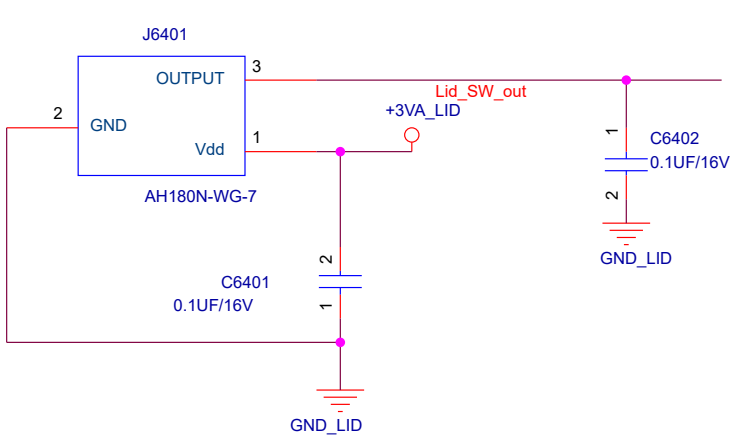
Project Name		Rev
ASUS GL752VW		1.0
Title : DC & BAT IN		
Size Custom	Dept.: ASUSTeK COMPUTER	Engineer: Wendell_Lo
Date: Wednesday, September 23, 2015	Sheet	60 of 102



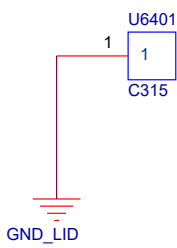
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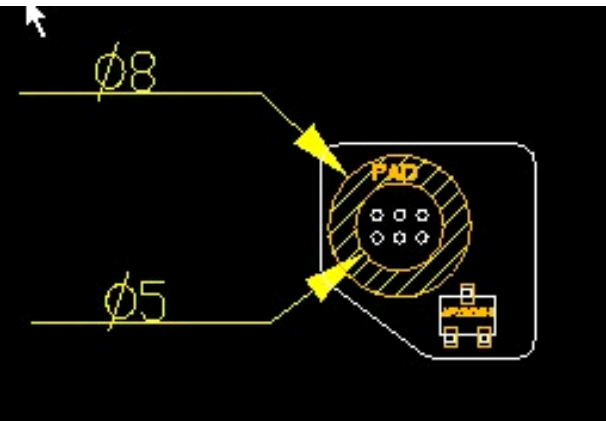
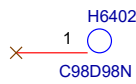
LID Switch



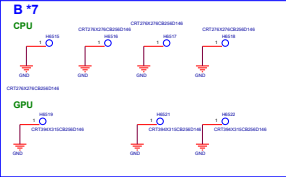
ME PAD



Hole



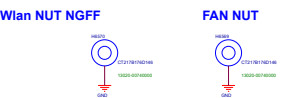
B*7



PCH NUT



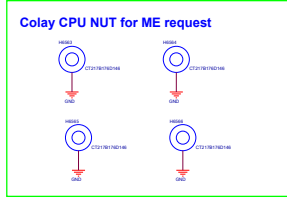
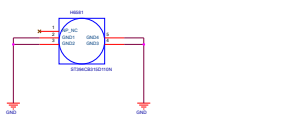
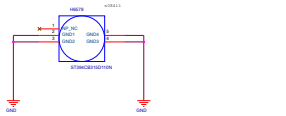
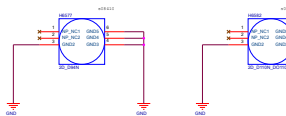
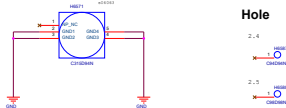
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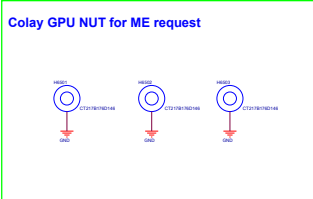
FAN NUT



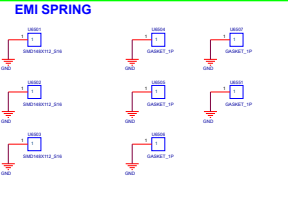
Hole



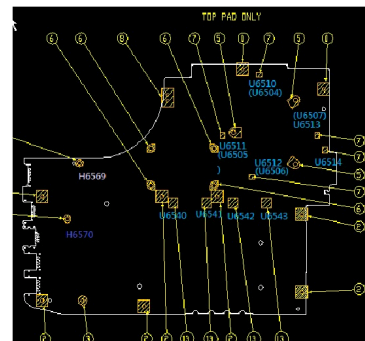
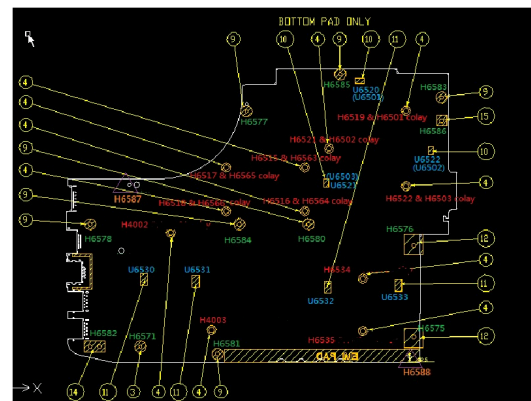
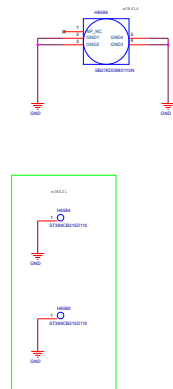
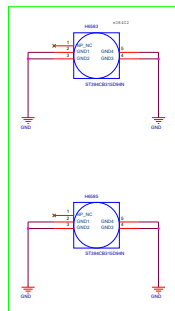
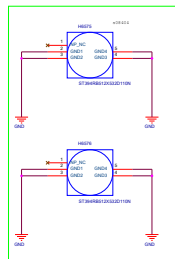
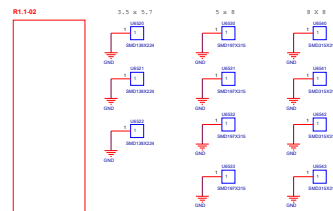
Colay GPU NUT for ME request



EMI SPRING



ME PAD



		Title : *****	
ASUSTek COMPUTER		Engineer: Wendell_Lo	
Size	Project Name	Rev	
B	GL752VW	1.0	
Date: Wednesday, September 23, 2015		Sheet	66 of 102



Title : *****

ASUSTeK COMPUTER

Engineer: **Wendell_Lo**

Size	Project Name
B	GL752VW

Rev
1.0

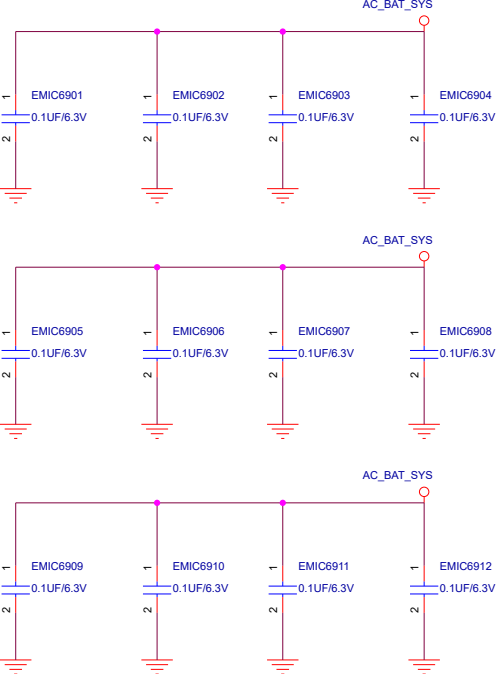


Title : OTH_for test only

ASUSTeK COMPUTER

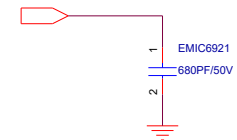
Engineer: Wendell_Lo

Size	Project Name	Rev
B	GL752VW	1.0



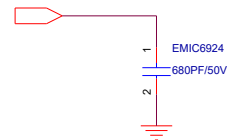
7,24,30,33,40,46,53,70

BUF_PLT_RST#



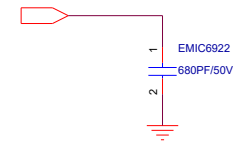
7,20,30,33

PM_RSMRST#



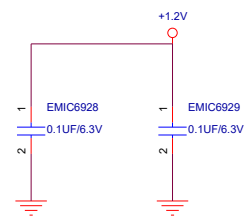
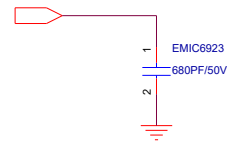
7,20,30,58,80

ALL_SYSTEM_PWRGD



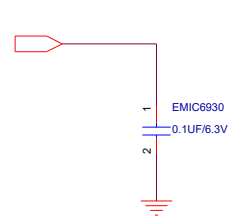
30,58

3VSUS_PWRGD



7,30,31,32

R1.0-36
PWR_SW#



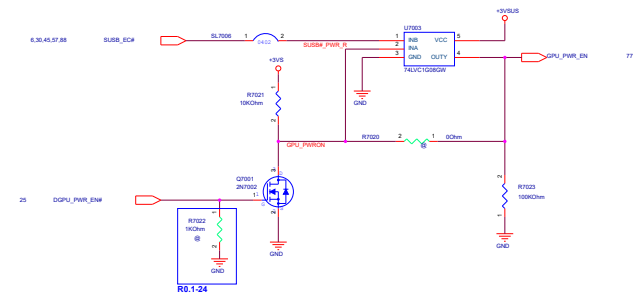
3	PCIEG_RXN[7:0]	
3	PCIEG_RXP[7:0]	
3	PCIEB_RXN[15:8]	
3	PCIEB_RXP[15:8]	



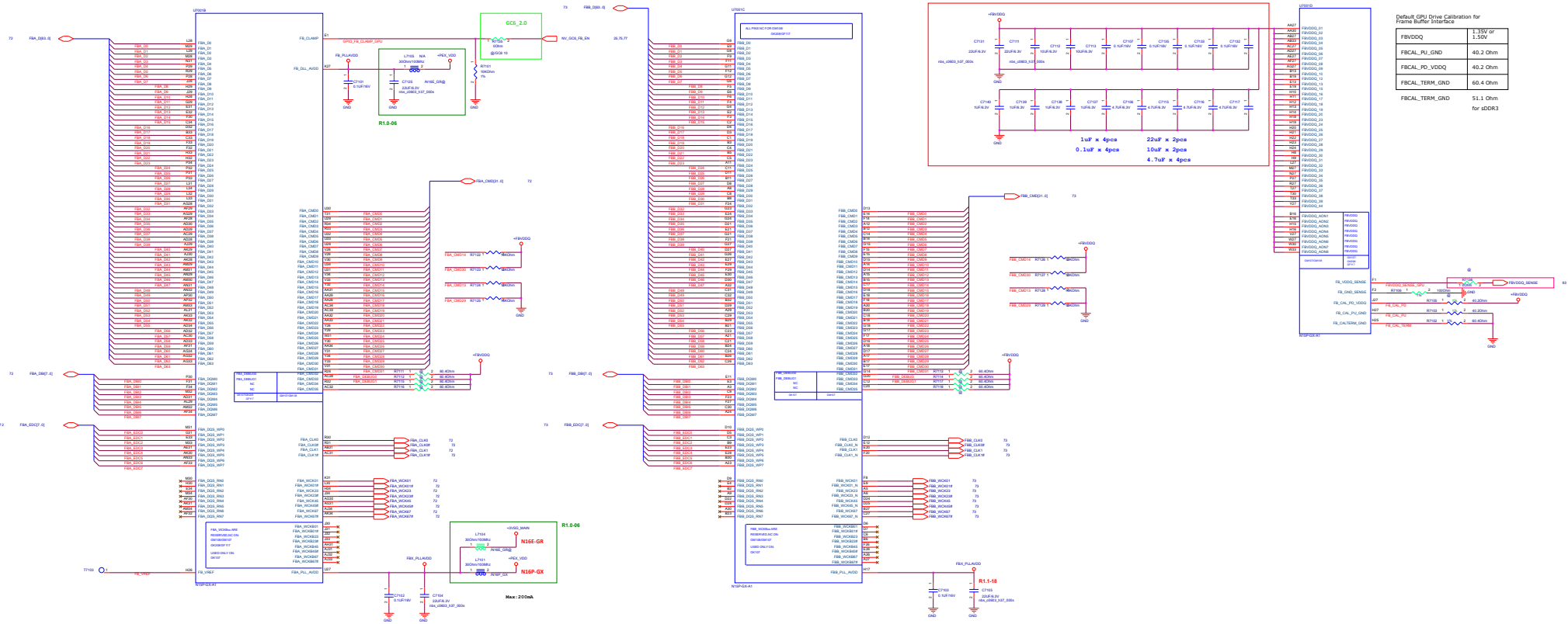
11



PEK LANE 6 TO 15 NO FOR GAC08GF117

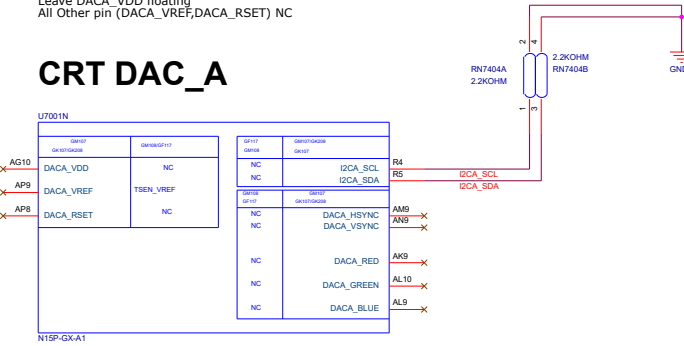


M7 Review 2014.11.12



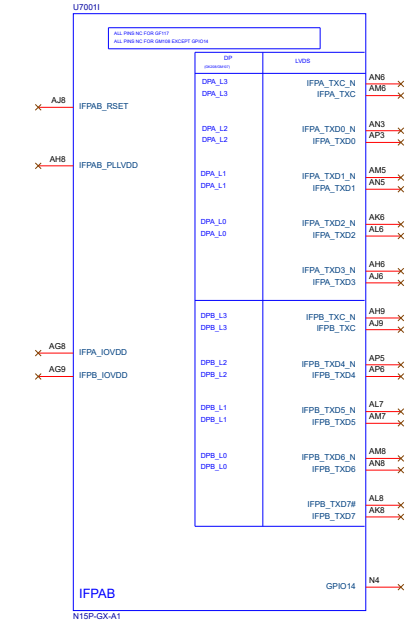
DG-06246-001_v04 DG9.6 p170
DAC interface not used
Leave DACA_VDD floating
All Other pin (DACA_VREF,DACA_RSET) NC
DG-06246-001_v02 DG10.2.1 p168
Unused I2C should be soft grounded or
PU 3.3V via 2.2kOhm

CRT DAC_A

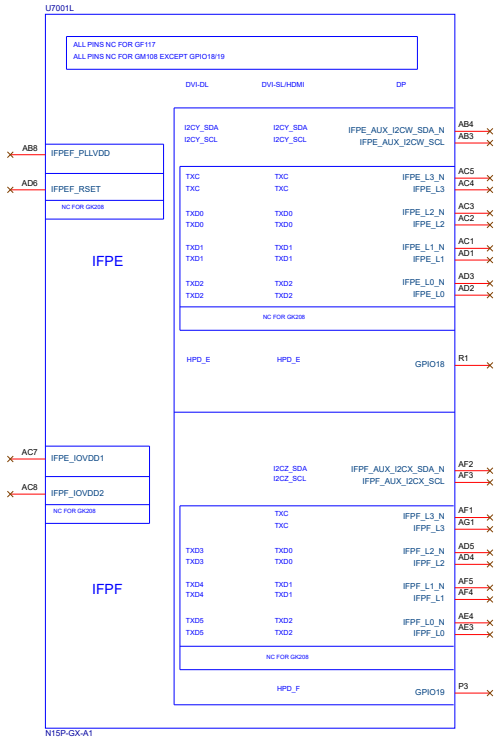


LVDS IFPA/B

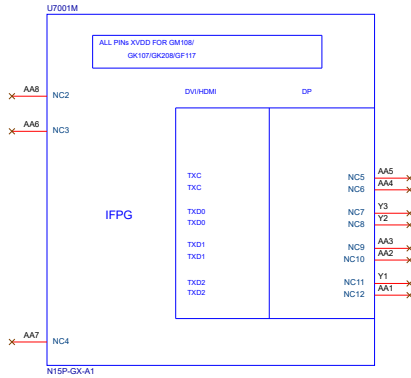
DG-06246-001_v04 DG8.6 p162
Float IFPxy_IOCDD/IFPxy_PLLVDD
Other pin NC



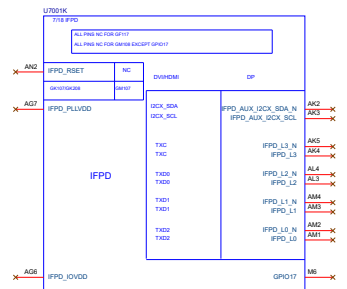
LVDS IFPE/F



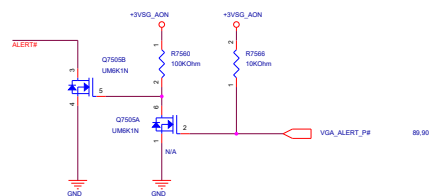
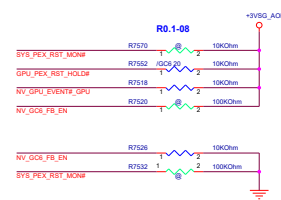
LVDS IFPG

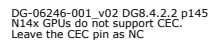


DG-06246-001_v02 p157 DG8.6
 IPF not used
 IFPxy_IOCDD/IFPxy_PLLVDD 10K PD
 Other pin NC

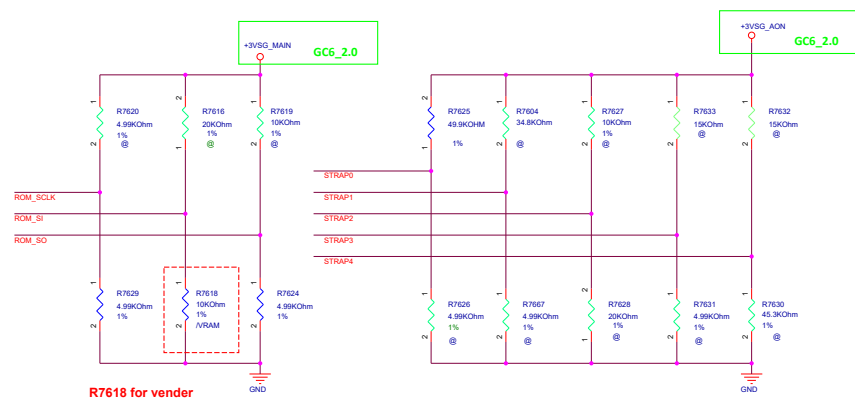


GPIO ASSIGNMENTS

[illegible]



STRAPPING OPTIONS for N16P



USE GDDR5 VRAM 128Mb x 32 (512MB)

Hynix strap 0x6 HYNIX/H5GC4H24AJR-T2C - 34.8Kohm +1.35V

Micron strap 0x4 Micron/EDW4032BABG-60-F - 24.9Kohm +1.35V

Samsung strap 0x3 Samsung/K4G41325FC-HC04 - 20Kohm +1.5V non-RVL

USE GDDR5 VRAM 128Mb x 32 (512MB)

1st: P/N: 03008-00030900 HYNIX/H5GC4H24AJR-T2C(A-die) ,Strap: 0x6 (+1.35V)

2nd: P/N: 03008-00030400 Micron/EDW4032BABG-60-F (A-die) ,Strap: 0x4 (+1.35V)

3nd: P/N: 03008-00030300 SAMSUNG/K4G41325FC-HC04 ,Strap: 0x3 (+1.5V, non-RVL)

	PU	PD
4.99K	1000	0000
10.0K	1001	0001
15.0K	1010	0010
20.0K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				

Table 7. N16P-GX GDDR5 Recommended Memories

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	128Mx16	Hynix	H5GC2H48FR-T2C	B-die	0x1	2500	1347	Production candidate
			Micron	EDW2032B8BG-6A-F	B-die	0x5	2500	N/A	Production candidate
			Samsung	K4G20325FD-FC03	D-die	0x0	2500	N/A	Production candidate
		256Mx16	Micron	EDW4032B8BG-60-F	A-die	0x4	2500	N/A	Production candidate
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production candidate
			Hynix	H5GC4H42MFR-T2C	M-die	0x2	2500	N/A	Production candidate

10uF x 2pcs



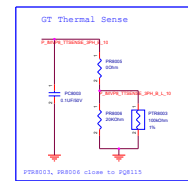


Title : SBU_DGPU_*****_R0.9

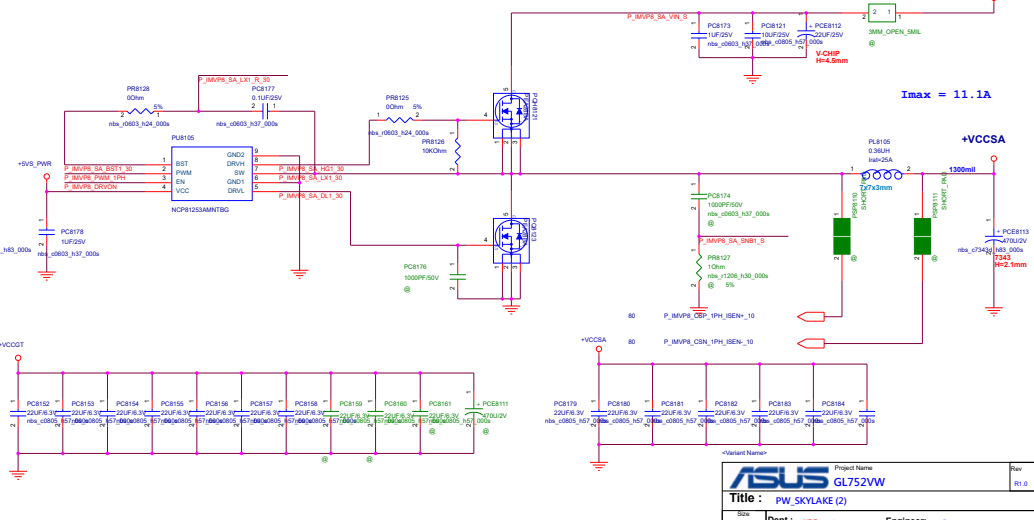
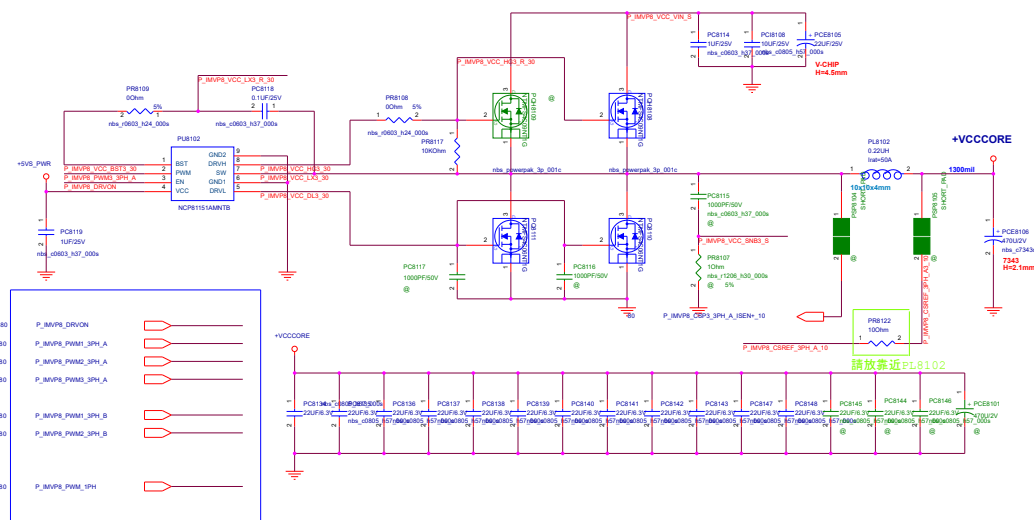
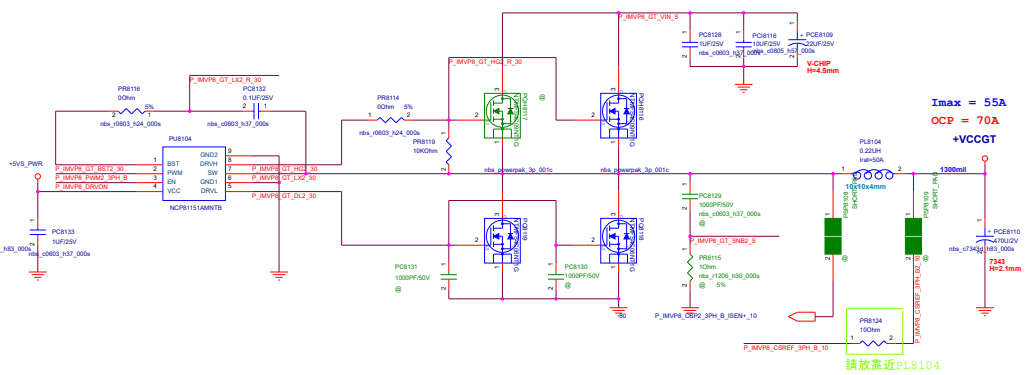
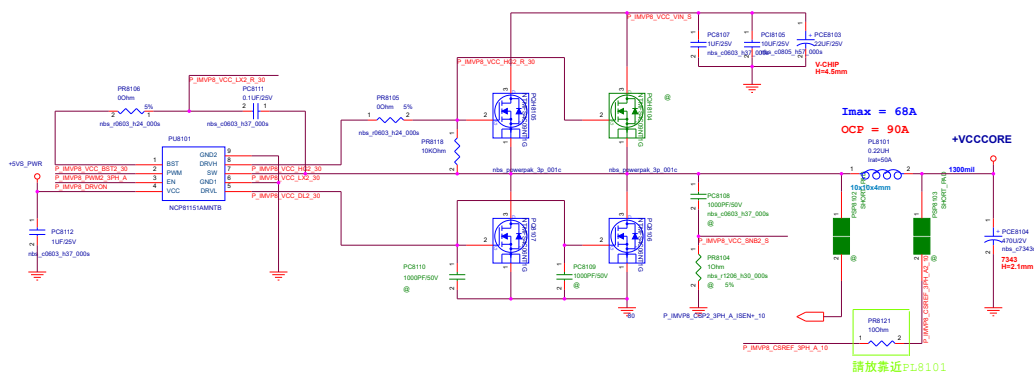
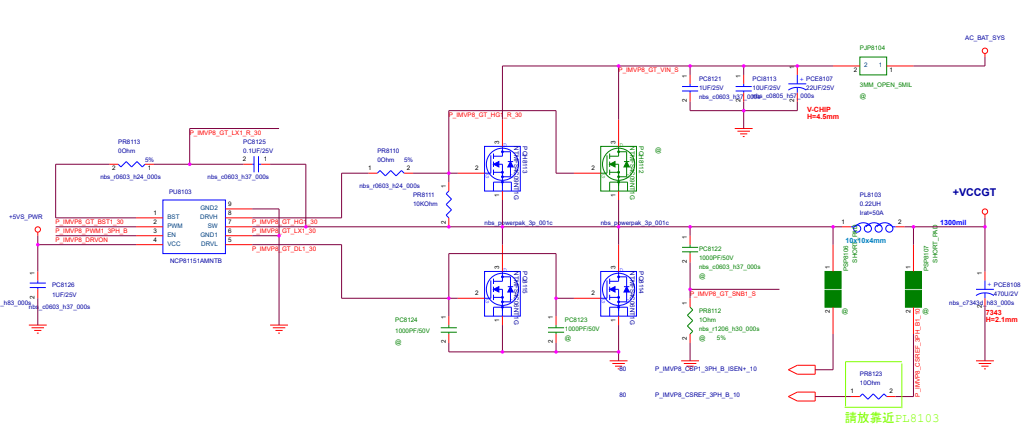
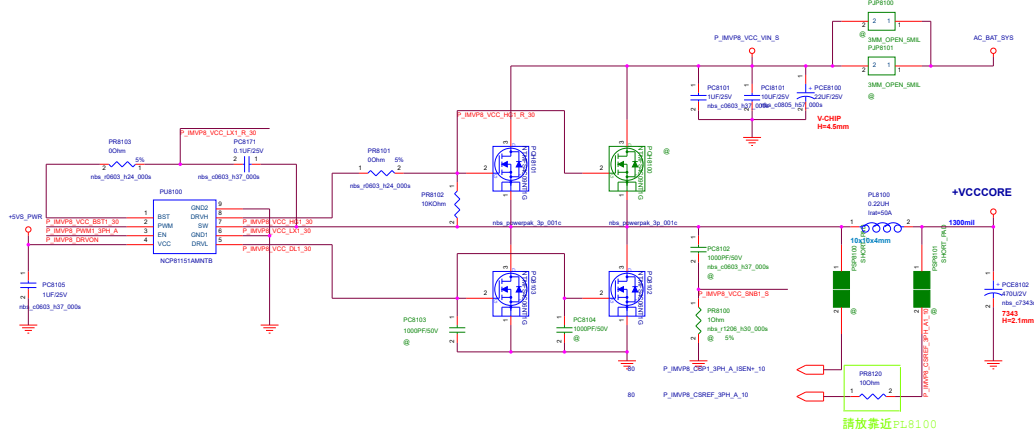
ASUSTeK COMPUTER

Engineer: Wendell_Lo

Size	Project Name	Rev
B	GL752VW	1.0



Skylake IMVP8 Power [For CPU]





Project Name

GL752VW

Rev

1.0

Title : PW_SKYLAKE (3)

Size

B

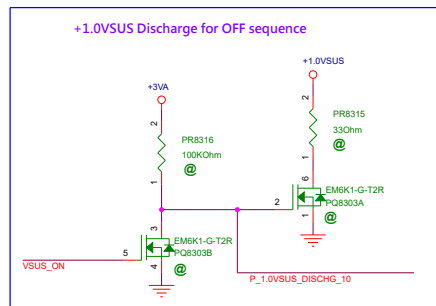
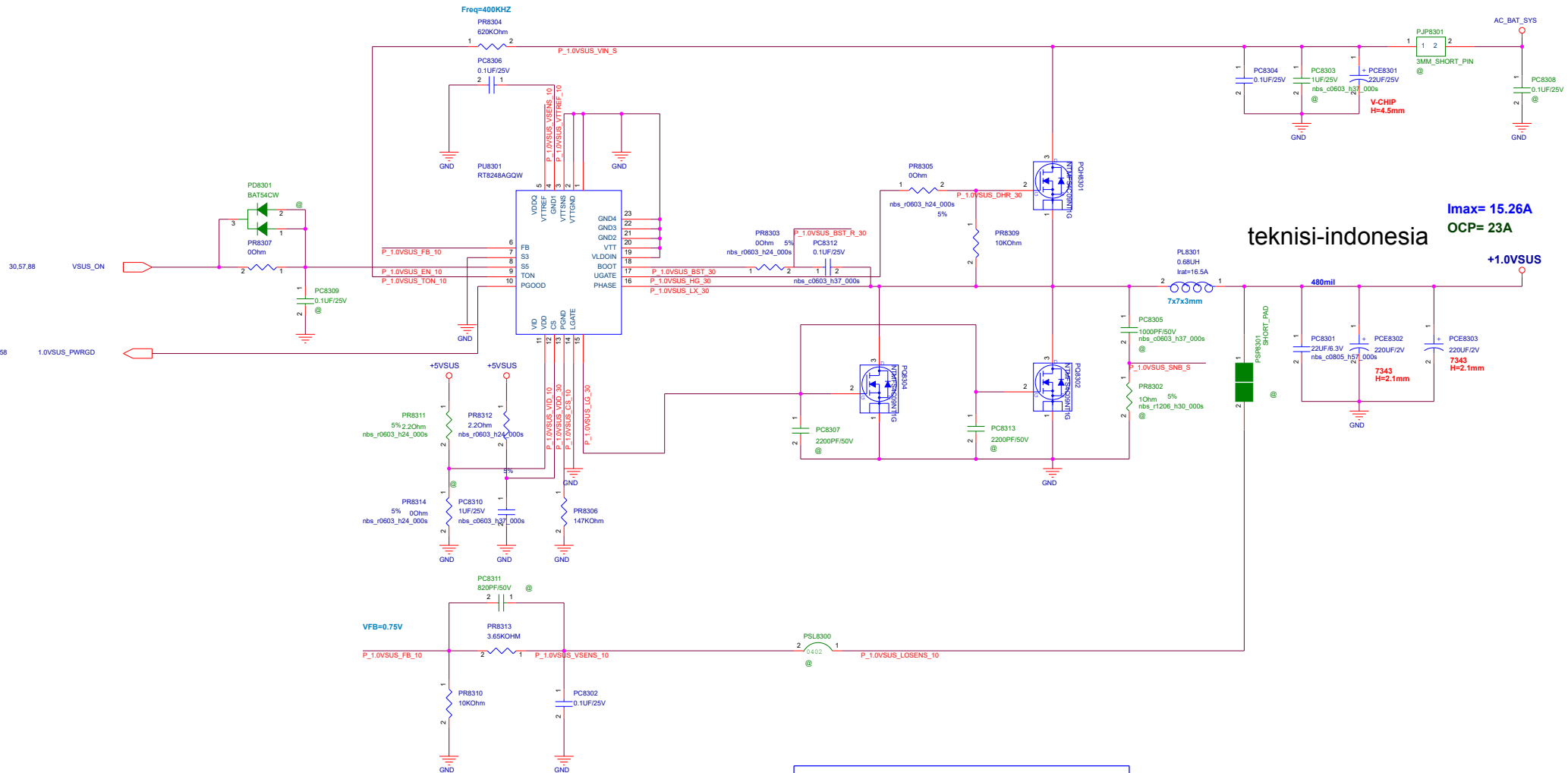
Dept.: NB Power team

Engineer: Joe

Date: Wednesday, September 23, 2015

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+1.0VSUS [For PCH]





Project Name

GL752VW

Rev

1.0

Title : PW_+VCCIO

Size

B

Dept.: NB Power team

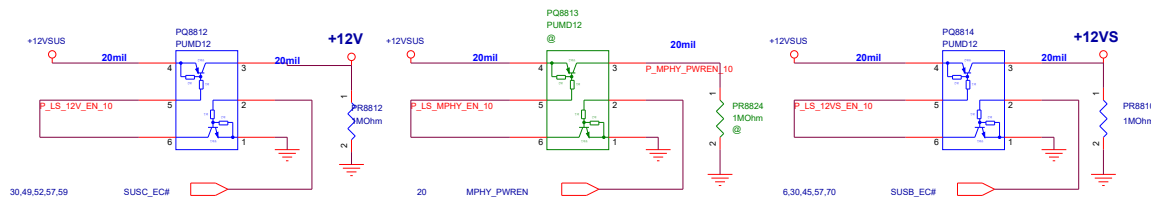
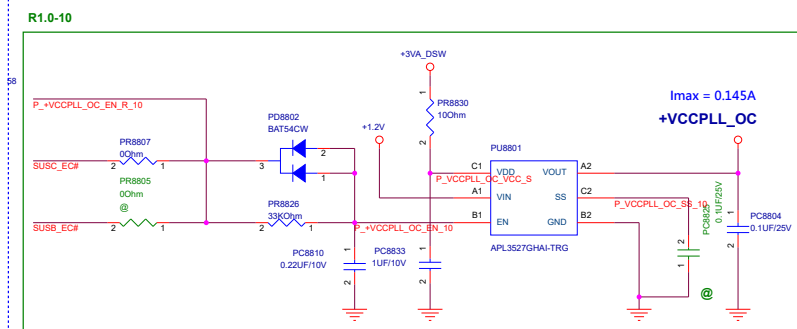
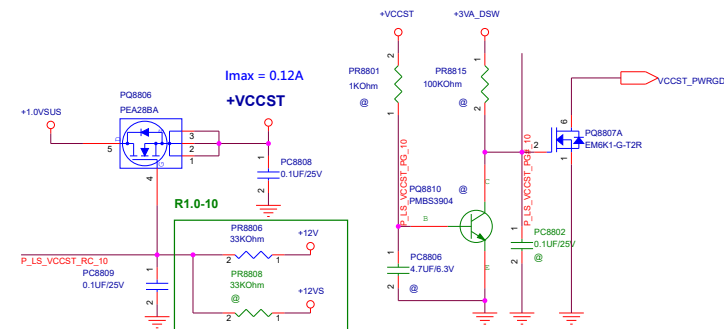
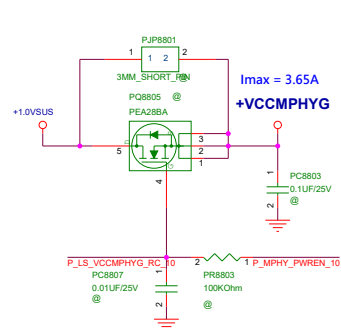
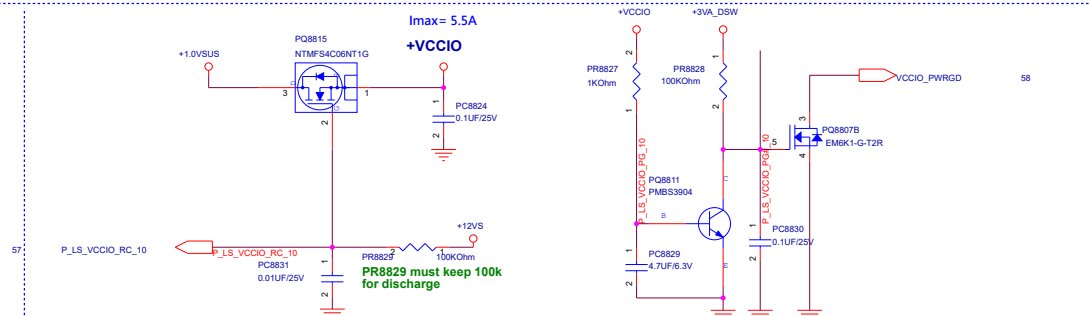
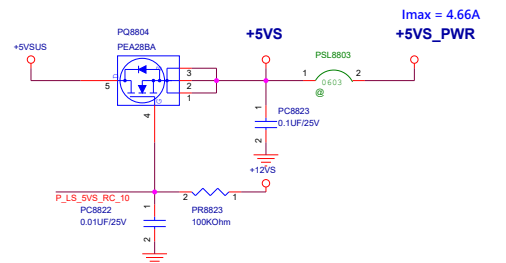
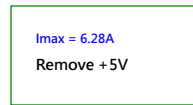
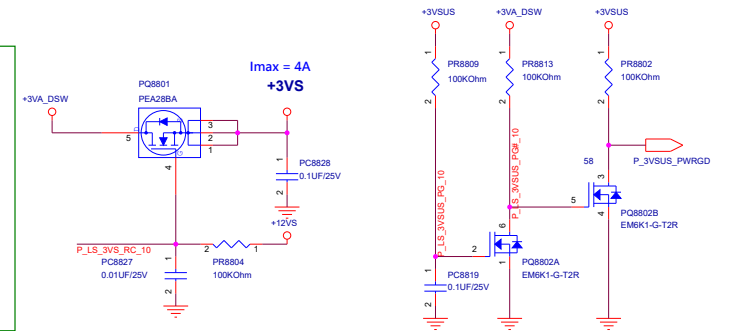
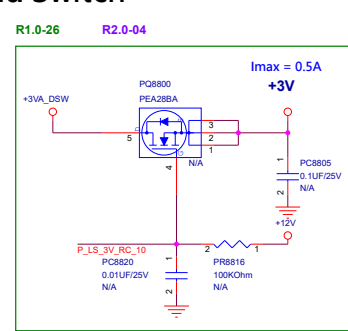
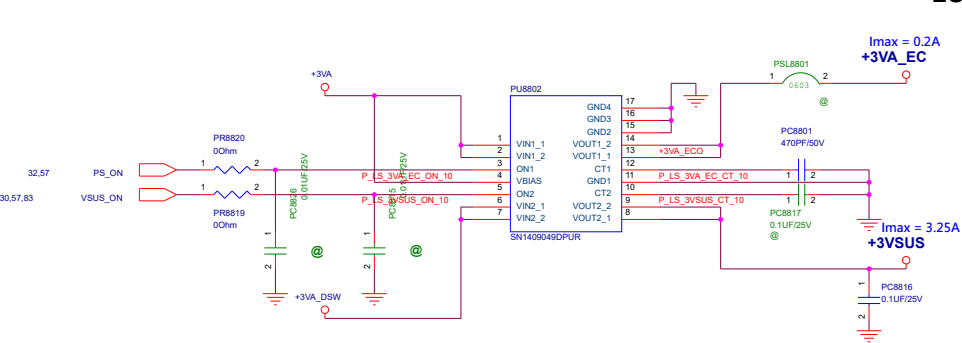
Engineer: Joe

Date: Wednesday, September 23, 2015

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		Project Name	Rev
		GL752VW	1.0
Title : POWER_+VGFX_CORE			
Size B	Dept.: NB Power team		Engineer: Joe
Date: Wednesday, September 23, 2015	Sheet	85	of 102

Load Switch



Address Selection Table

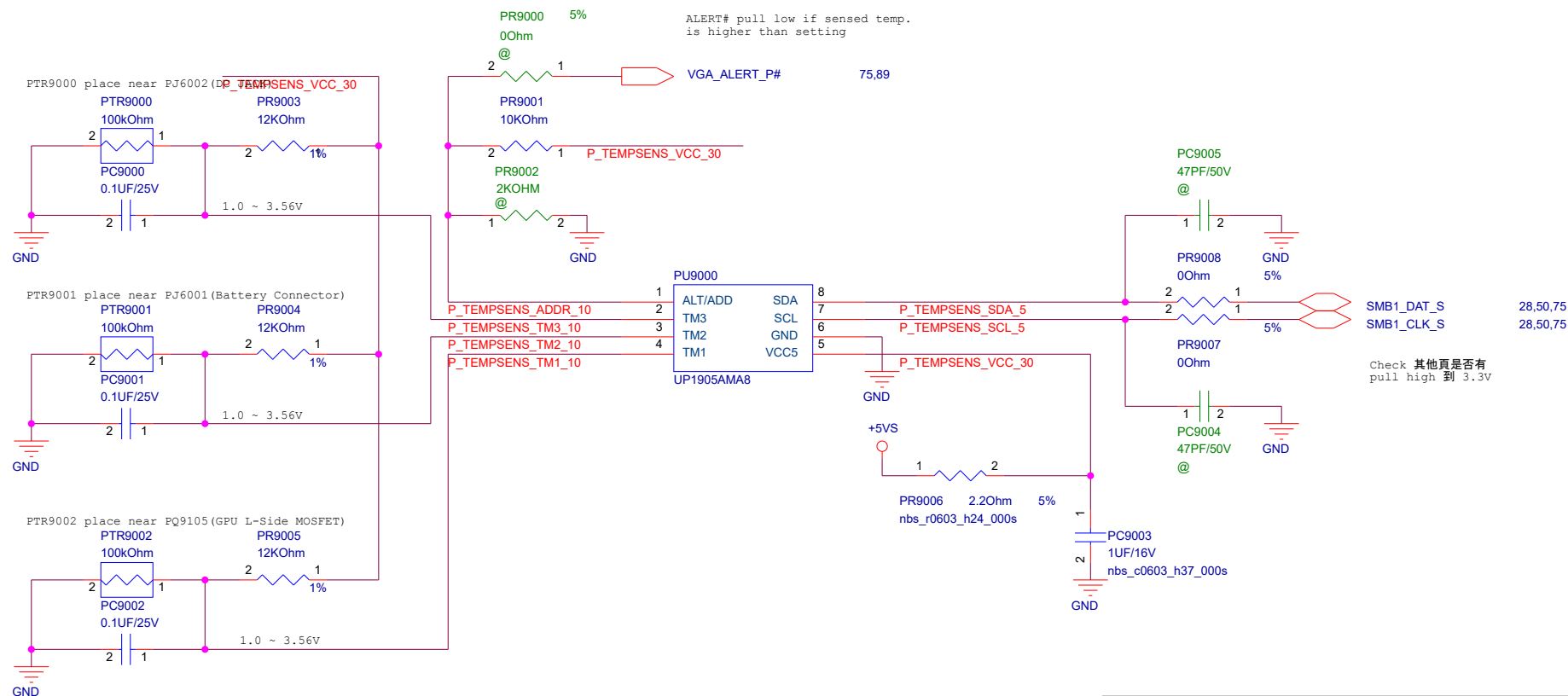
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9404	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9405	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Main	2nd
------	-----

Register Address

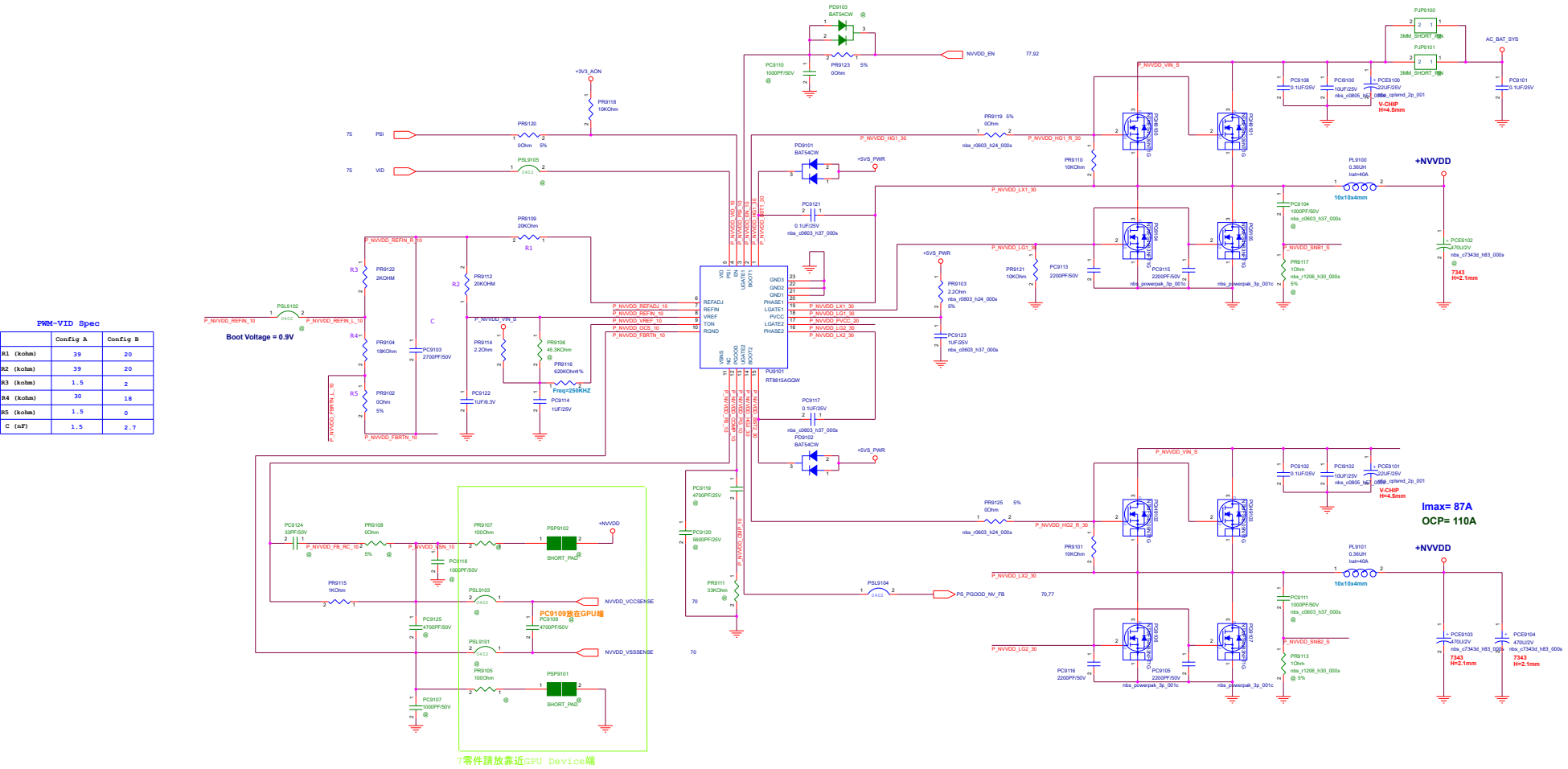
Address	0x00 0x01 0x02	0x03 0x04 0x05	0x06
R/W	W W W	R R R	R
Function	Temp. alert threshold setting	Sensed temp. data	bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

Main Board

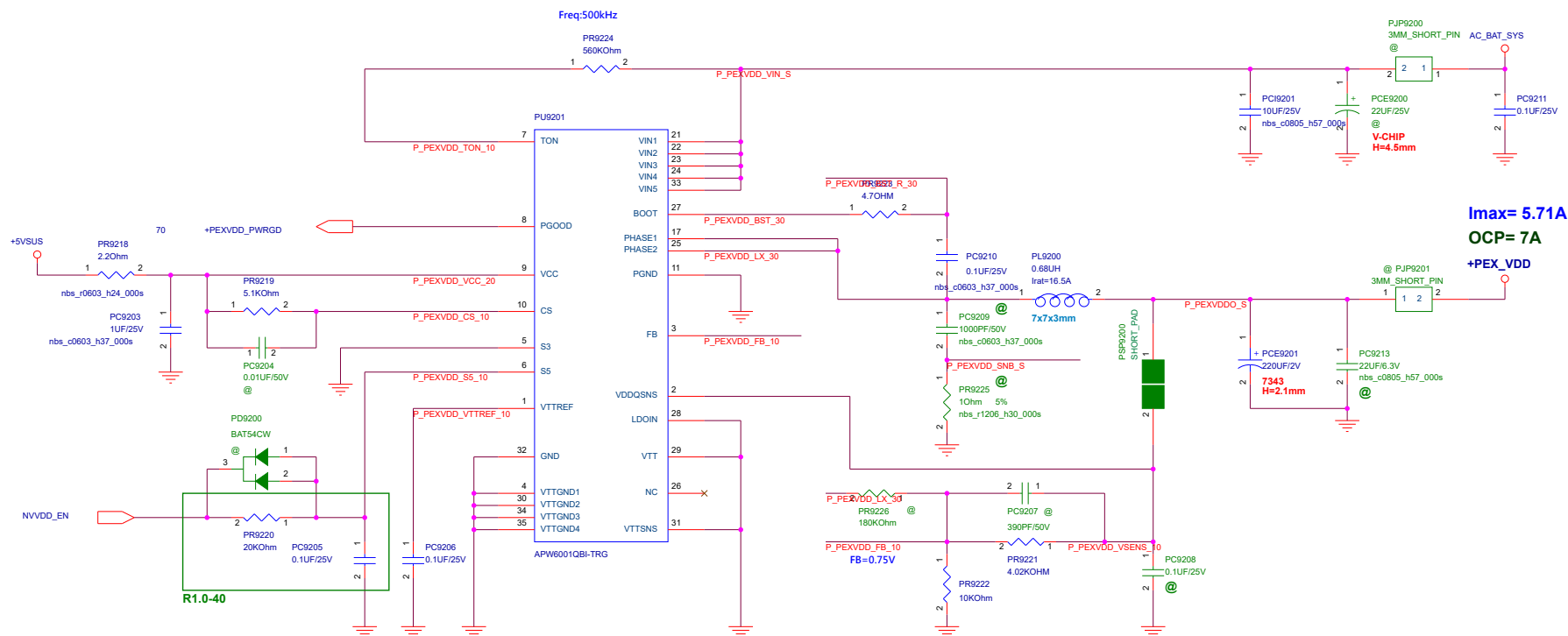


		Project Name GL752VW		Rev 1.0	
Title : PW_PROTECTION					
Size Custom		Dept.: NB Power team		Engineer: Joe	
Date: Wednesday, September 23, 2015				Sheet 90 of 102	

+NVVDD [For DGPU]



+PEX_VDD [For DGPU]



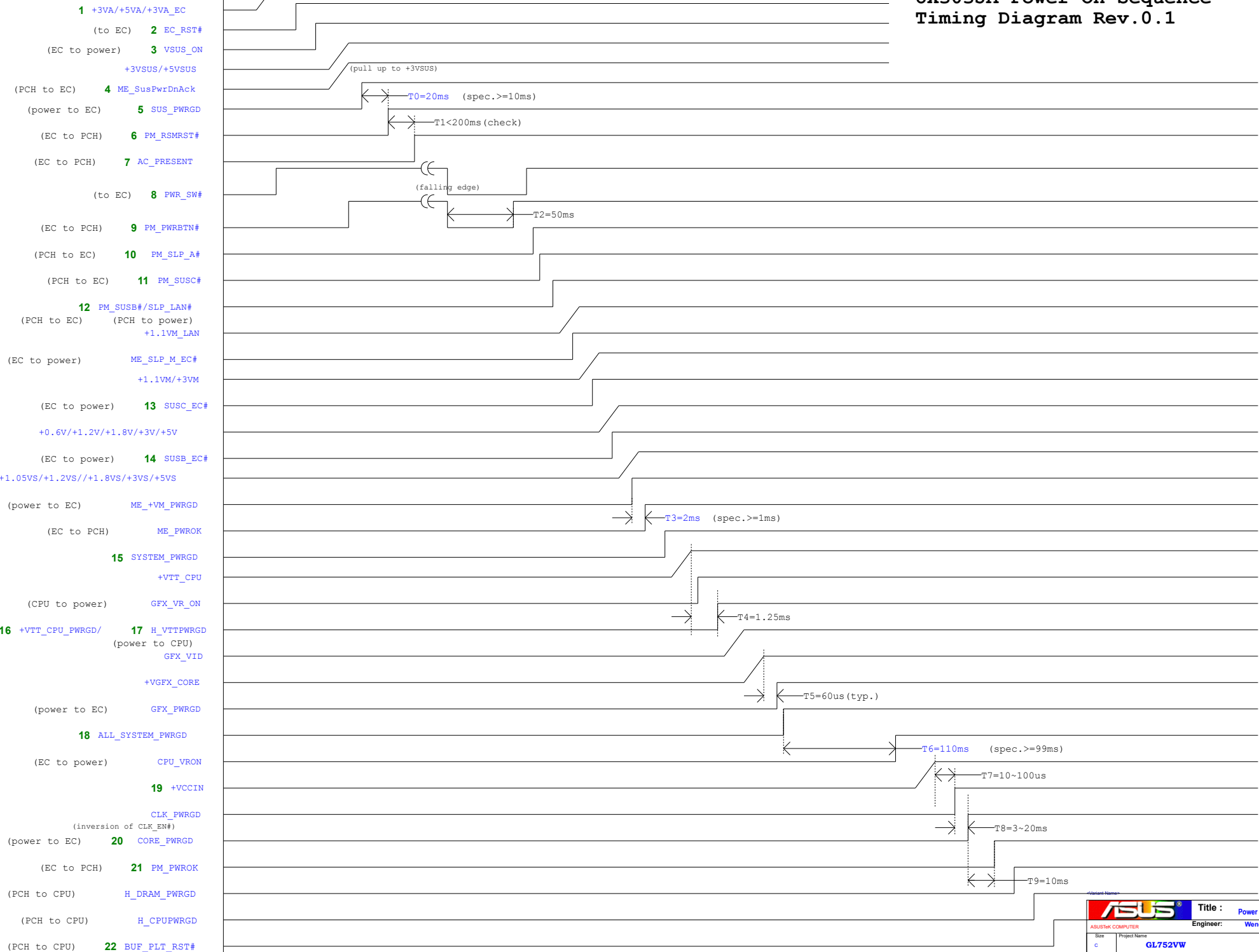
PR9221	UP1740_Q_Vout
3.6kohm	1.0V
4.02kohm	1.05V
6.2kohm	1.2V
8.2kohm	1.35V
10.5kohm	1.5V

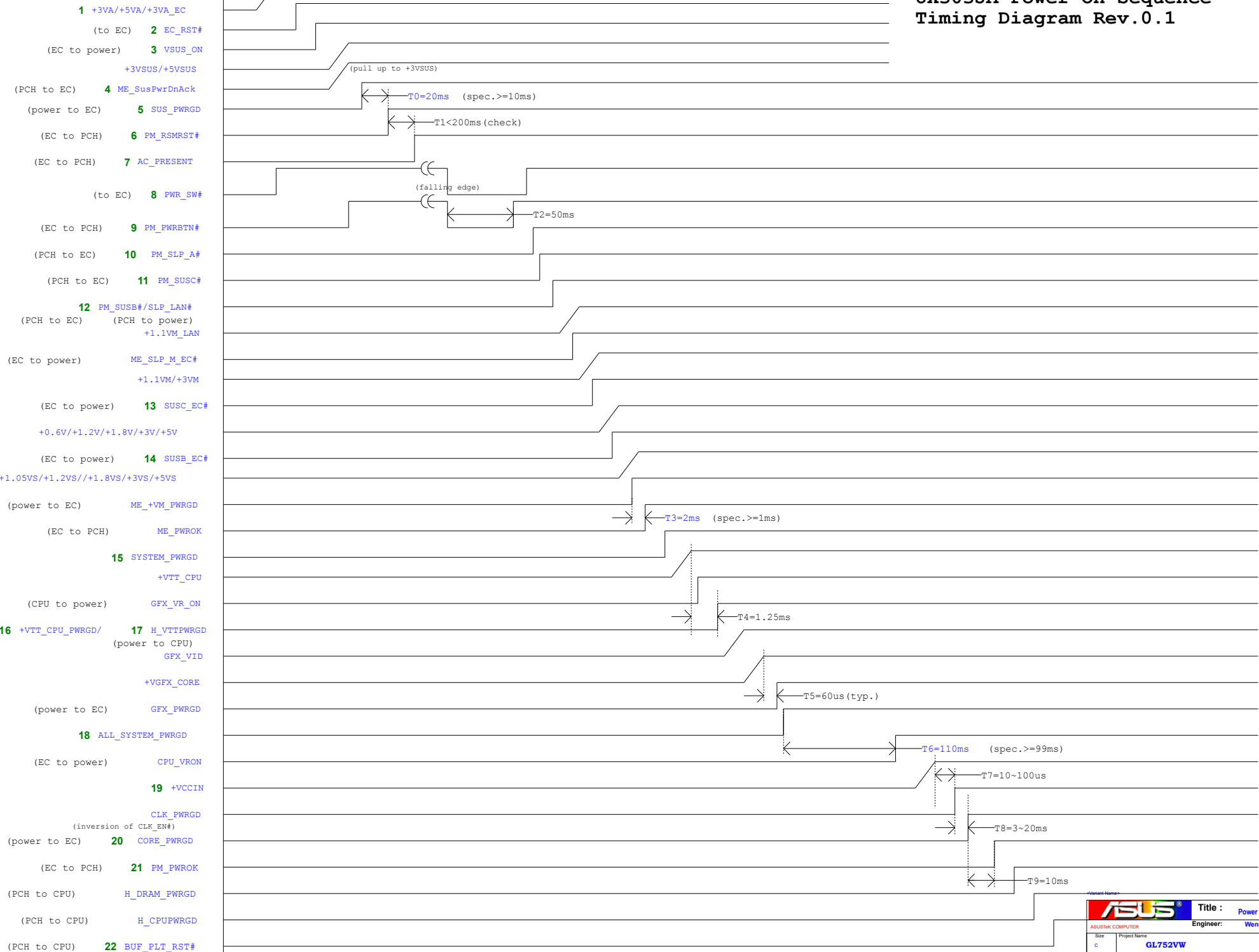
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		GL752VW	1.0
Title : PW_THUNDERBOLT			
Size			
B	Dept.: NB Power team	Engineer:	Joe
Date: Wednesday, September 23, 2015		Sheet	94 of 102

		Project Name	Rev
		GL752VW	1.0
Title : POWER_+VGFX_CORE			
Size	Dept.:	Engineer:	
B	NB Power team	Joe	
Date:	Wednesday, September 23, 2015	Sheet	95 of 102

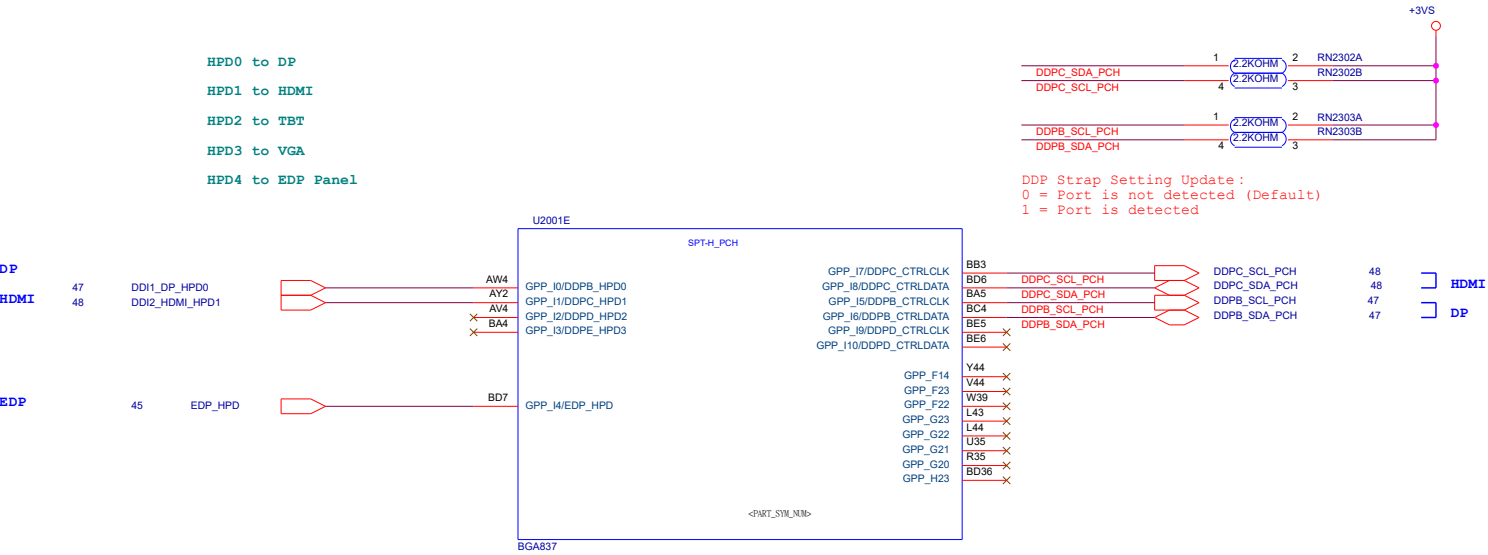
		Project Name	Rev
		GL752VW	1.0
Title : POWER_+VGFX_CORE			
Size			
B	Dept.: NB Power team	Engineer:	Joe
Date: Wednesday, September 23, 2015	Sheet	96	of 102

		Project Name	Rev
		GL752VW	1.0
Title : PW_OV			
Size			
B	Dept.: NB Power team	Engineer:	Joe
Date: Wednesday, September 23, 2015	Sheet	97	of 102



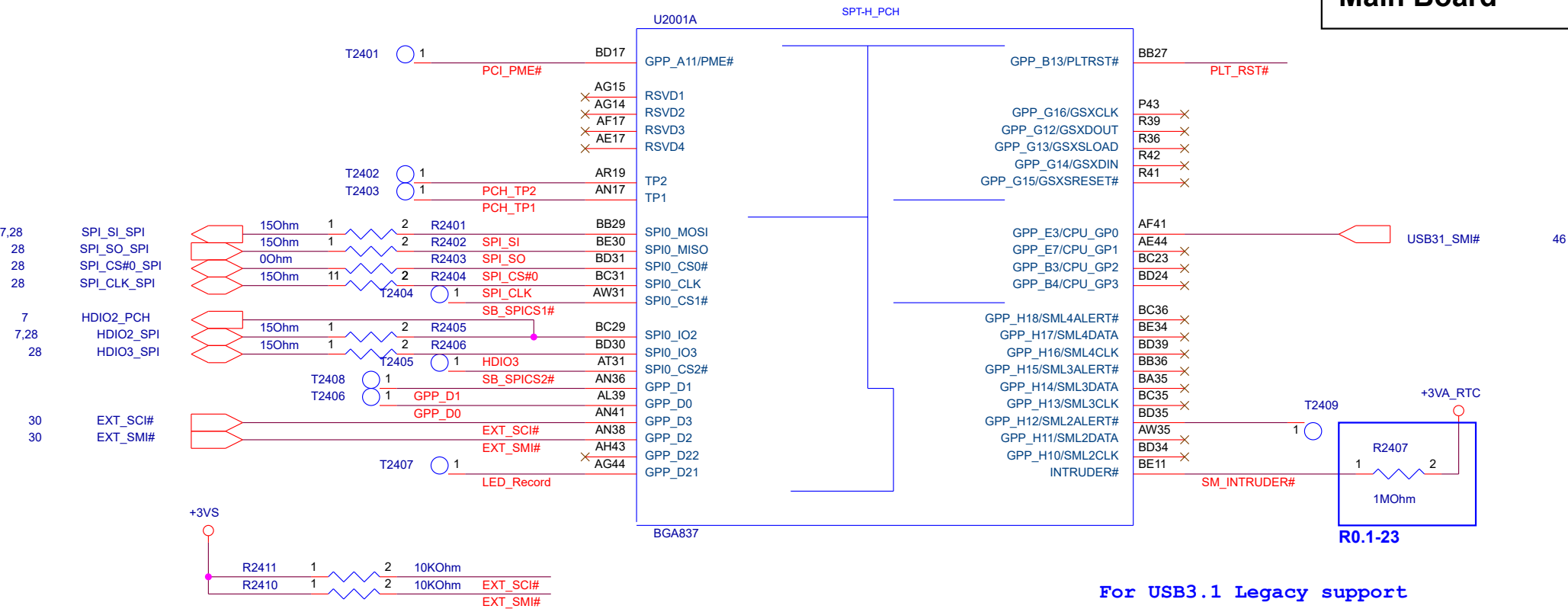


	Title : Revision History	
	Engineer: Wendell_Lo	
L752VW		Rev 1.0

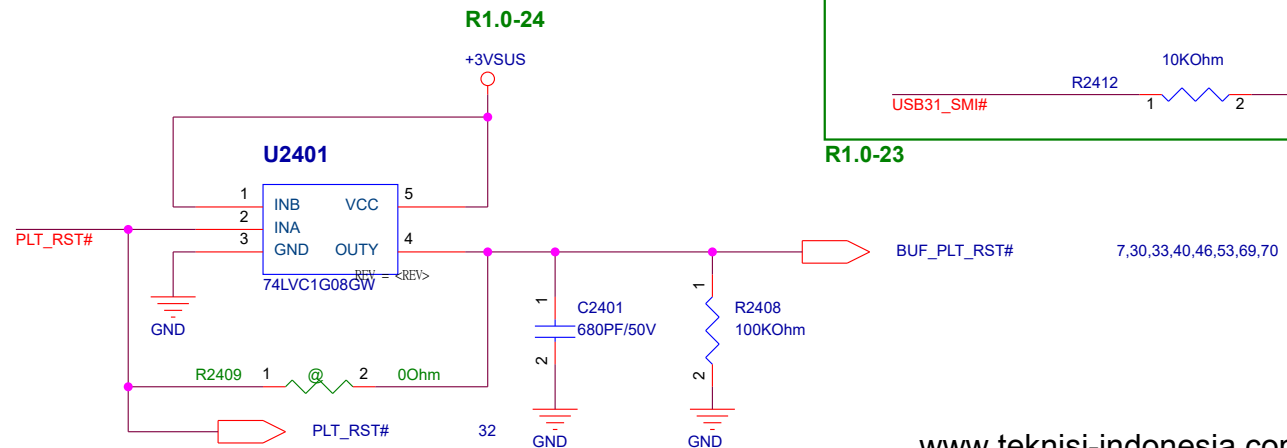
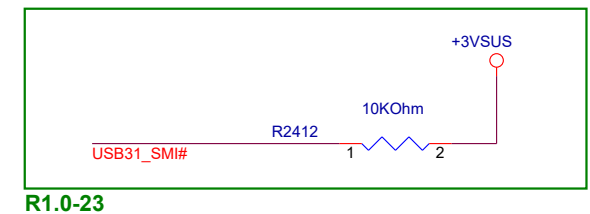


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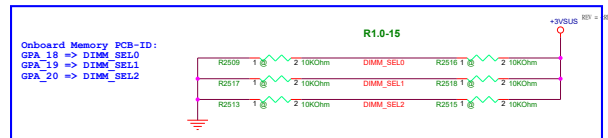
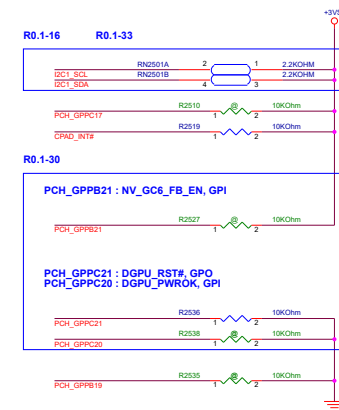
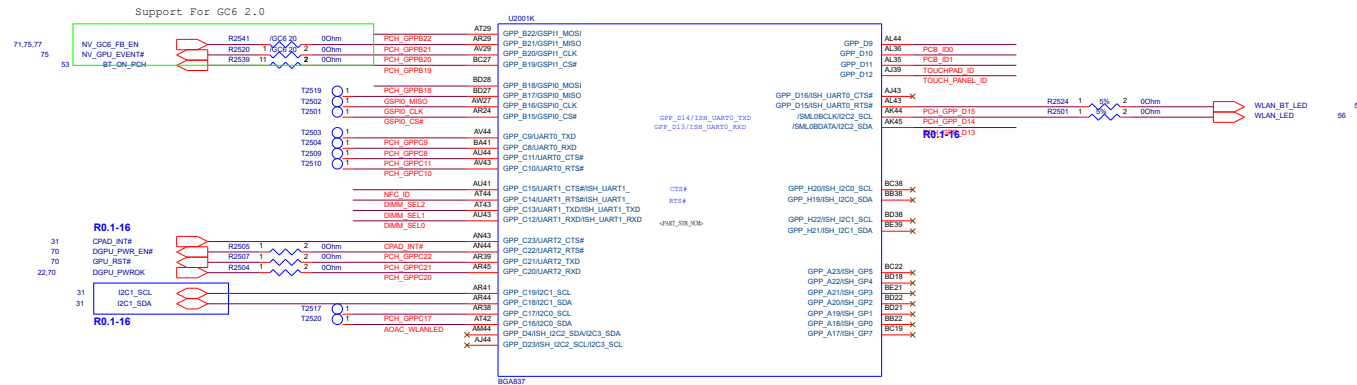
Main Board



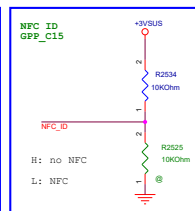
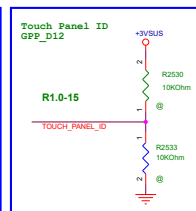
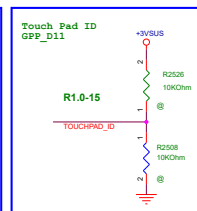
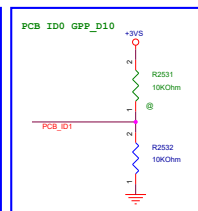
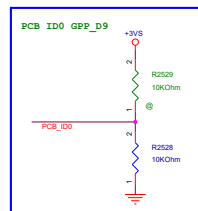
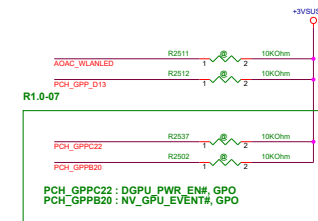
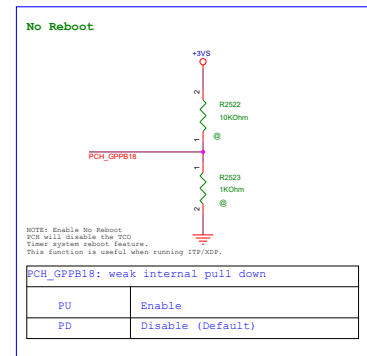
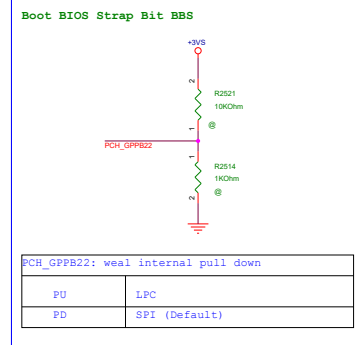
For USB3.1 Legacy support

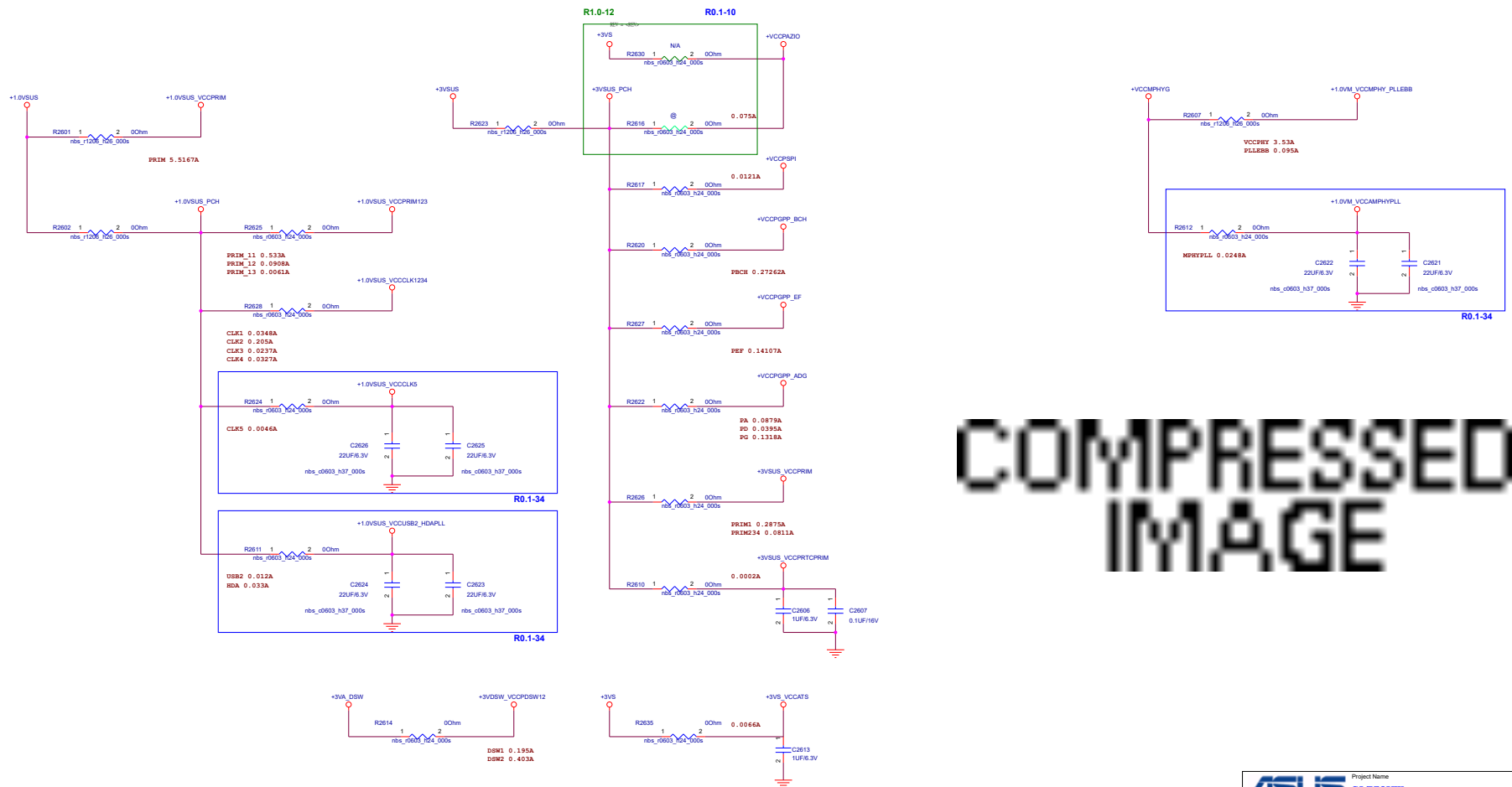
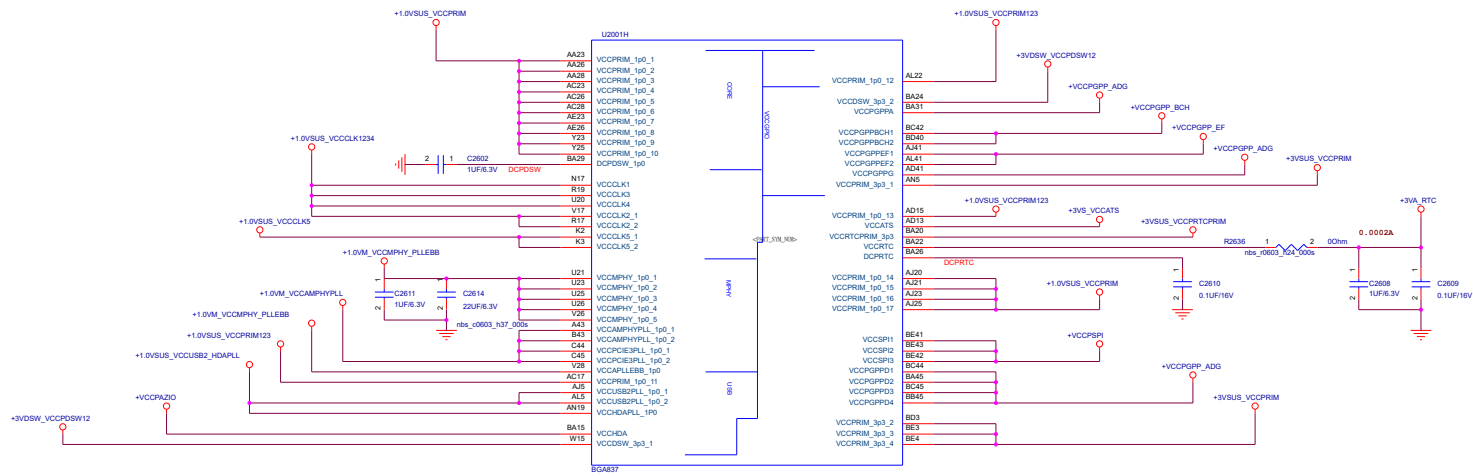


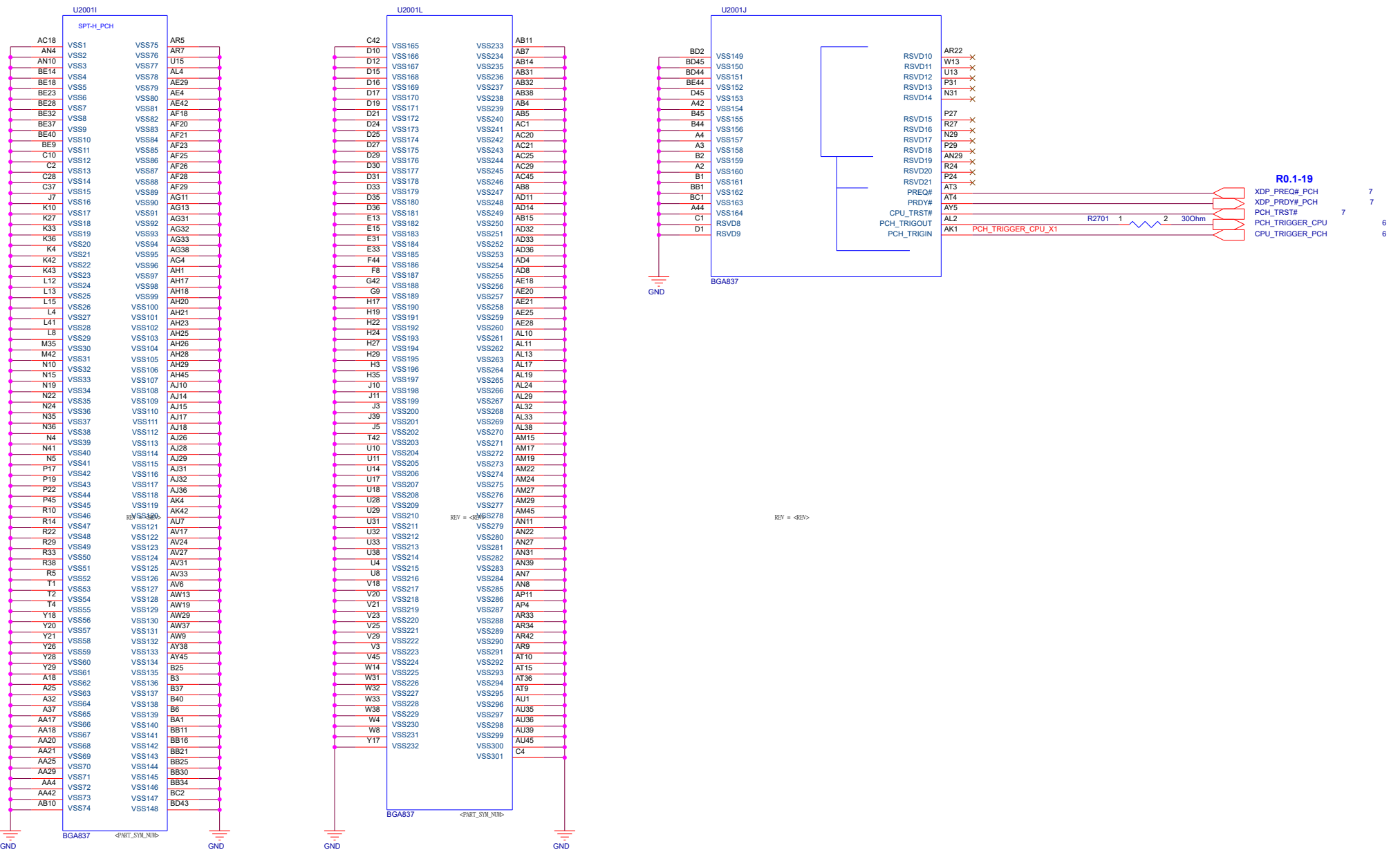
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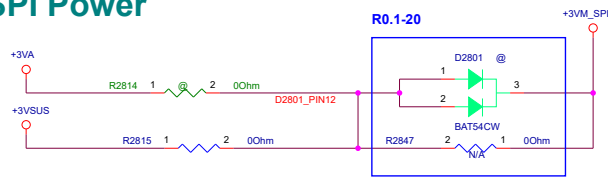
	DIMM SLOT	MEM DOWN	MEM DOWN	MEM DOWN
DIMM_SEL0				
DIMM_SEL1				
DIMM_SEL2				





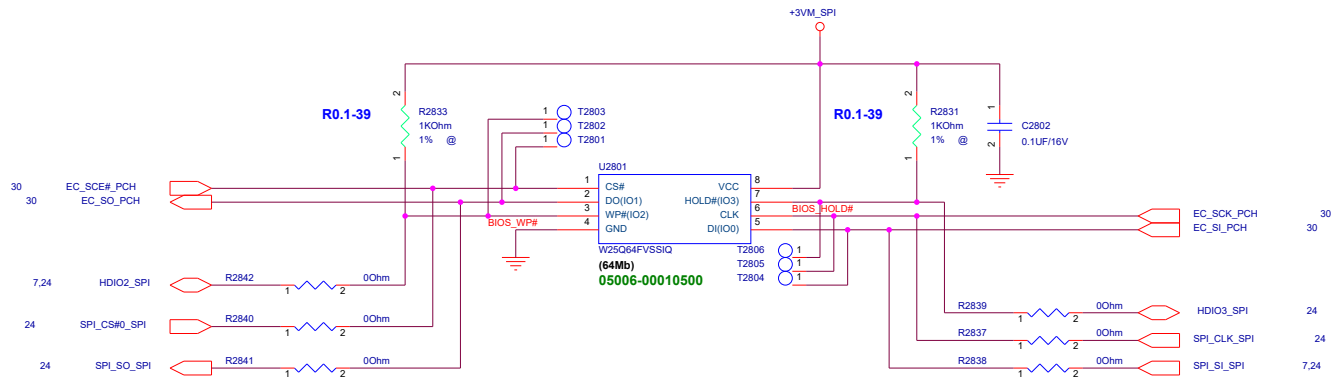


SPI Power

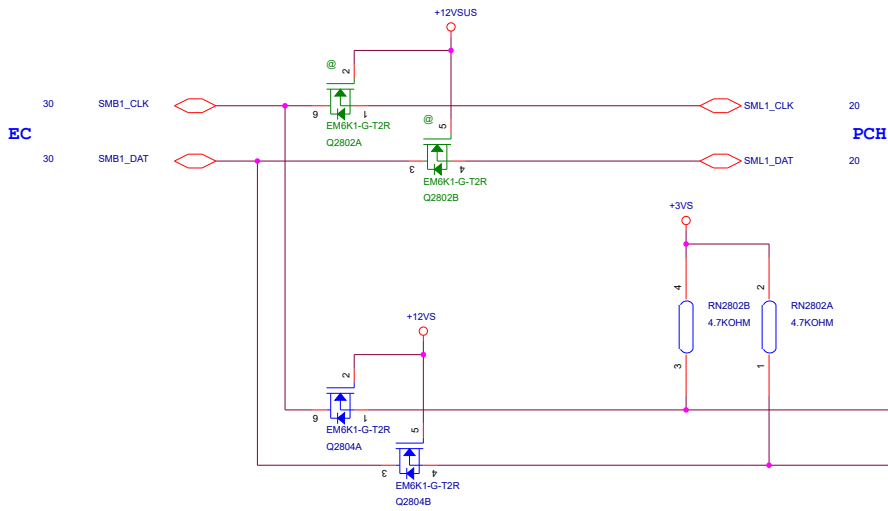


1st SPI ROM

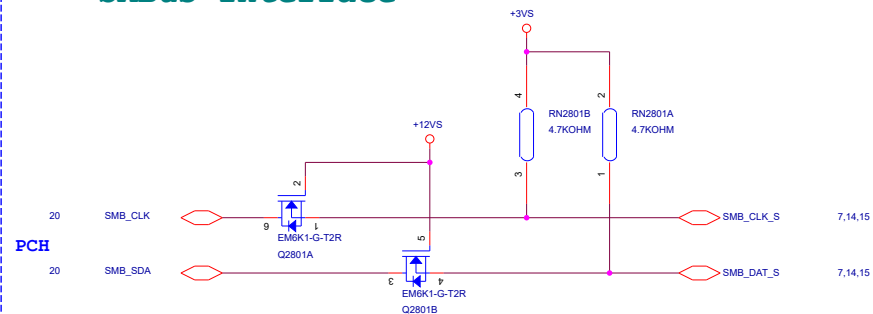
Main: 05006-00010500 (fixed quad bit)



System Management Interface



SMBus Interface



R0.1-13 R1.0-01

CPU,VGA Thermal Sensor
Power Thermal Sensor

		Project Name GL752VW		Rev 1.0
Title : PCH-XDP				
Size B	Dept.: ASUSTeK COMPUTER		Engineer:	Wendell_Lo
Date: Wednesday, September 23, 2015			Sheet 29	of 102

Only 3V Torrence

GPB[0,1,2,3,4,5,6]
GPC[3,4,5,6,7]
GPD[0,4,6,7]
GPE[4]
GPF[6,7]
GPH[7]
GPI [0 : 7]
GPJ [0 : 7]

Can be adjusted to
Open-Drain for port:

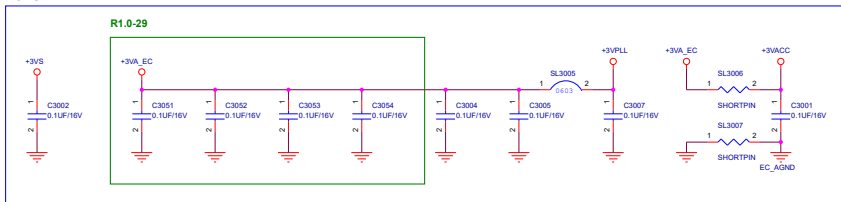
GPB0-GPA3
GPB0-GPB7
GPD0-GPD7
GPE0-GPE7
GPF0-GPF7
GPH0-GPH6
GPJ0-GPJ5

EC Require

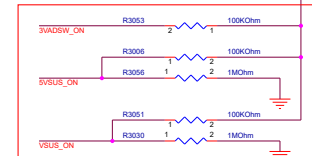
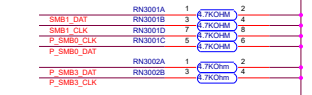
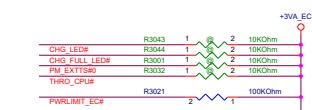
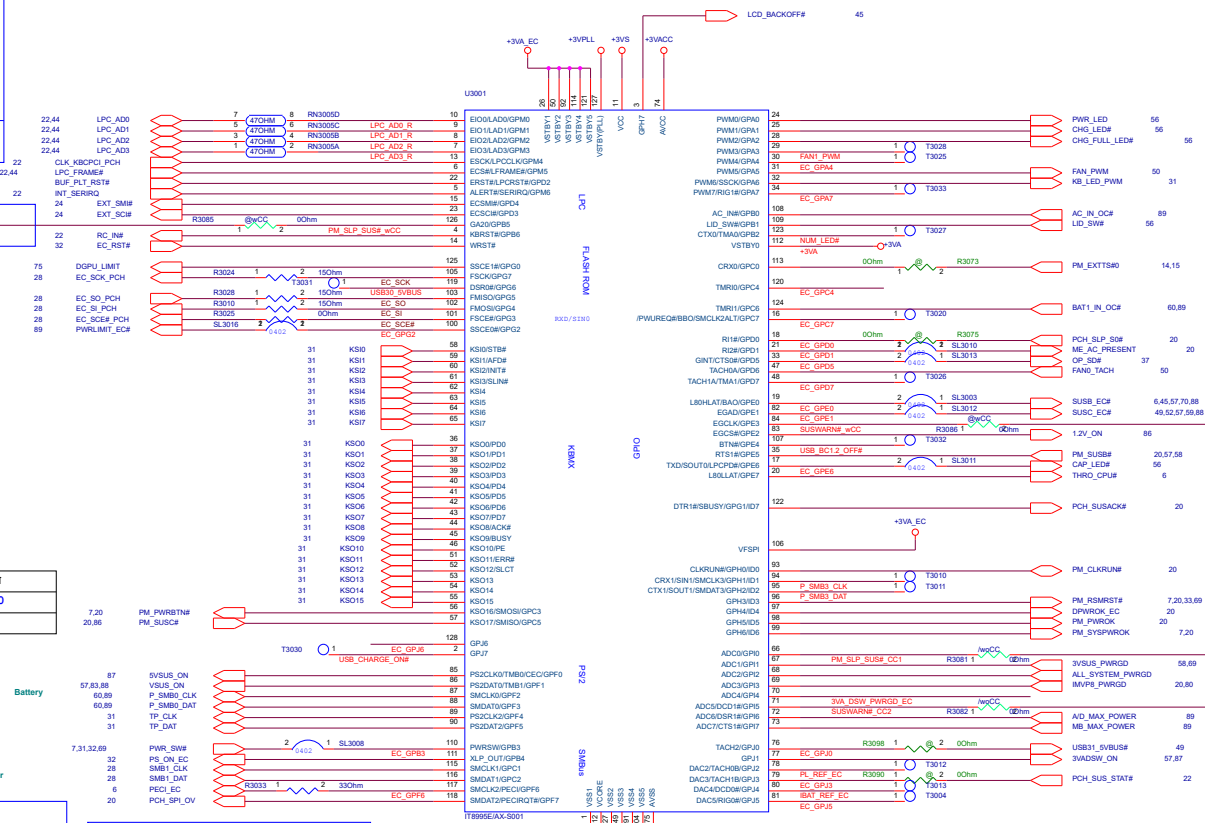
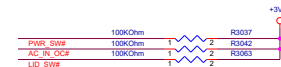
R0.1-41

ITE Version	ASUS P/N
IT8995E/AX	06037-00050400

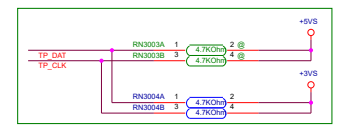
Power



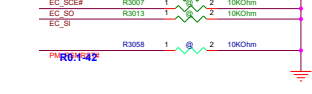
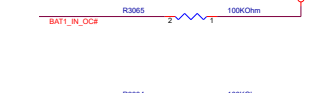
PU/PD



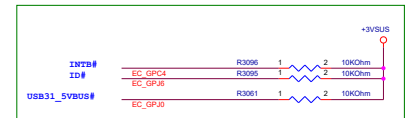
for load code



ClickPad Schematic



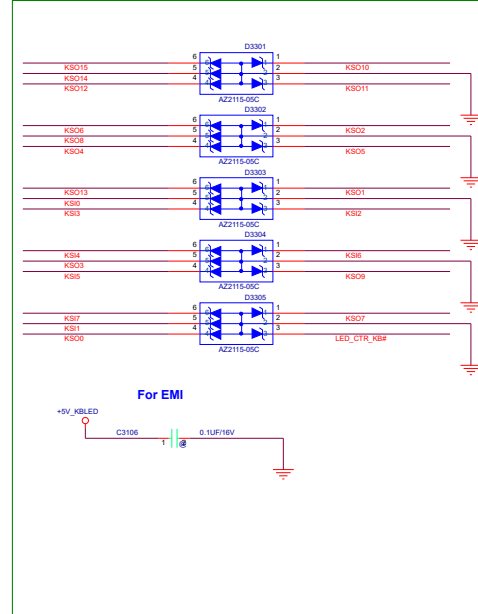
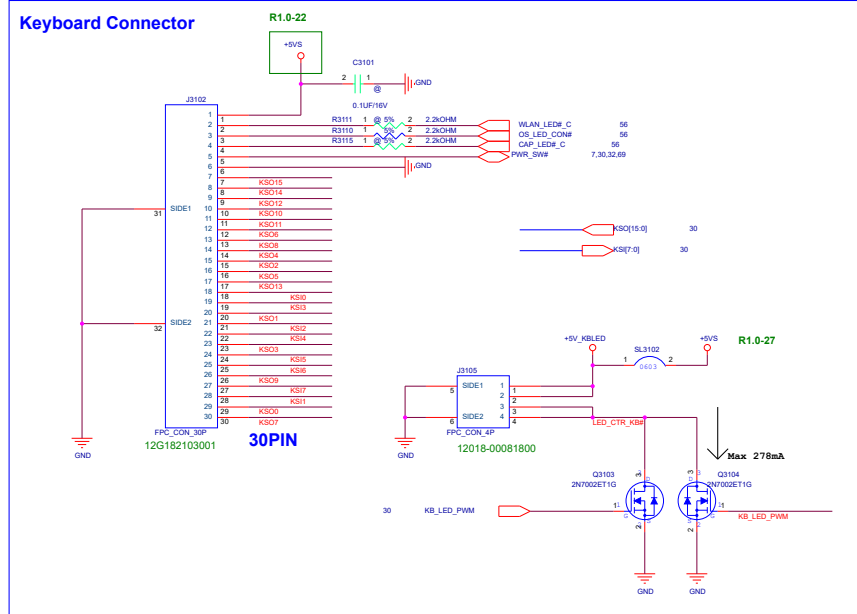
To CC logic at p49



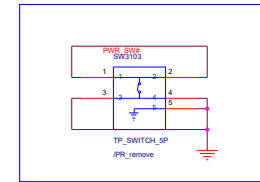
<Variant Name>

ASUS		Title : CR_KBC.IT8521	
ASUSTek COMPUTER		Engineer: Wendell_Lo	
Size	Project Name	GL752VW	
Date	Wednesday, September 23, 2015	Sheet	30 of 102

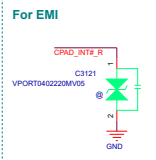
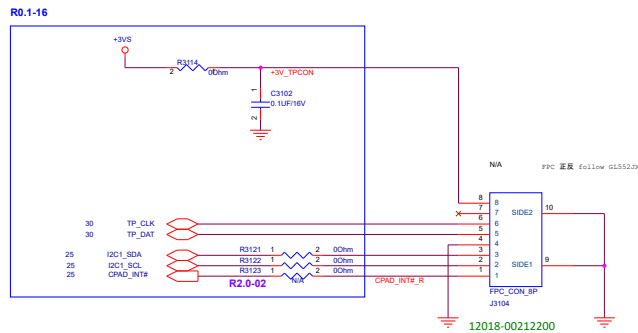
Keyboard Connector



POWER button for SR

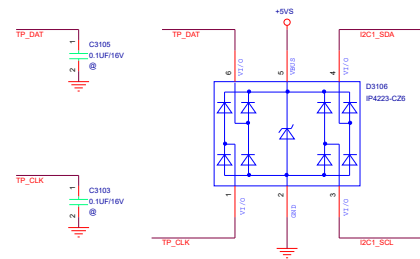


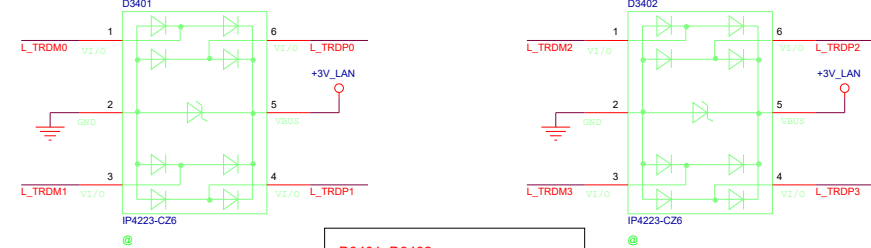
Click touch Pad Connector



R1.1 pin define reverse for ME request

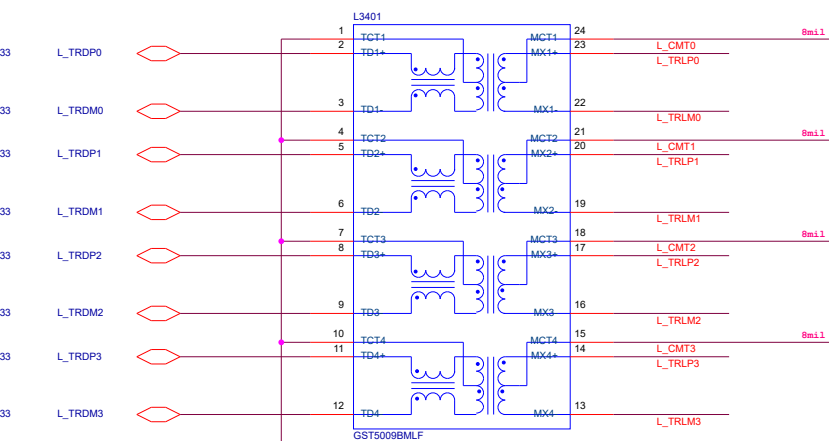
Reserved for EMI



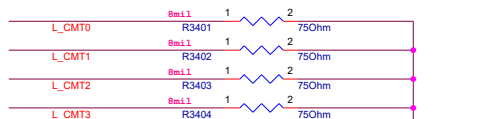


D3401, D3402
家電下鄉改用
AMAZING AZ1013-04S
07G028161010

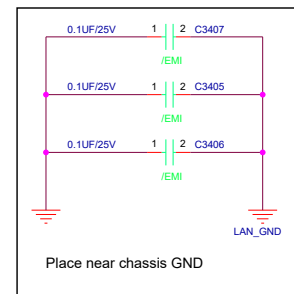
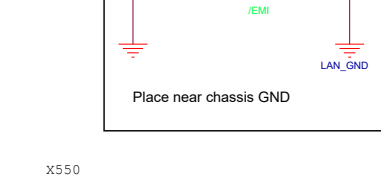
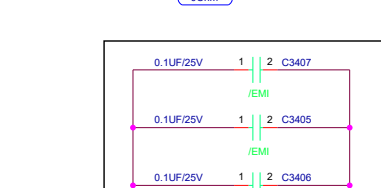
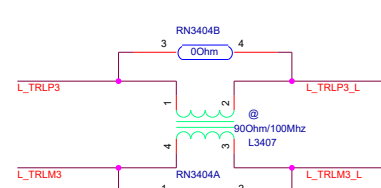
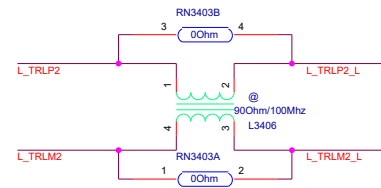
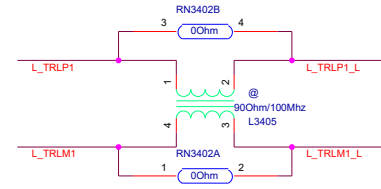
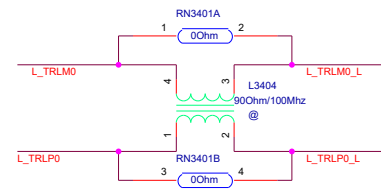
D3401, D3402 pin2
need 2 GND Vias.



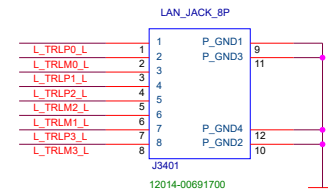
1st source: 09G051059640
2nd source: 09G051059055
3rd source: 09G051059A20
4th source: 09G051059A30



X550



Place near chassis GND



Change GND TO LAN_GND FOR EMI



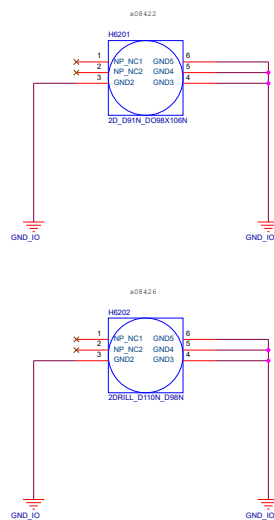
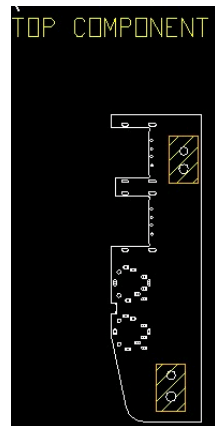
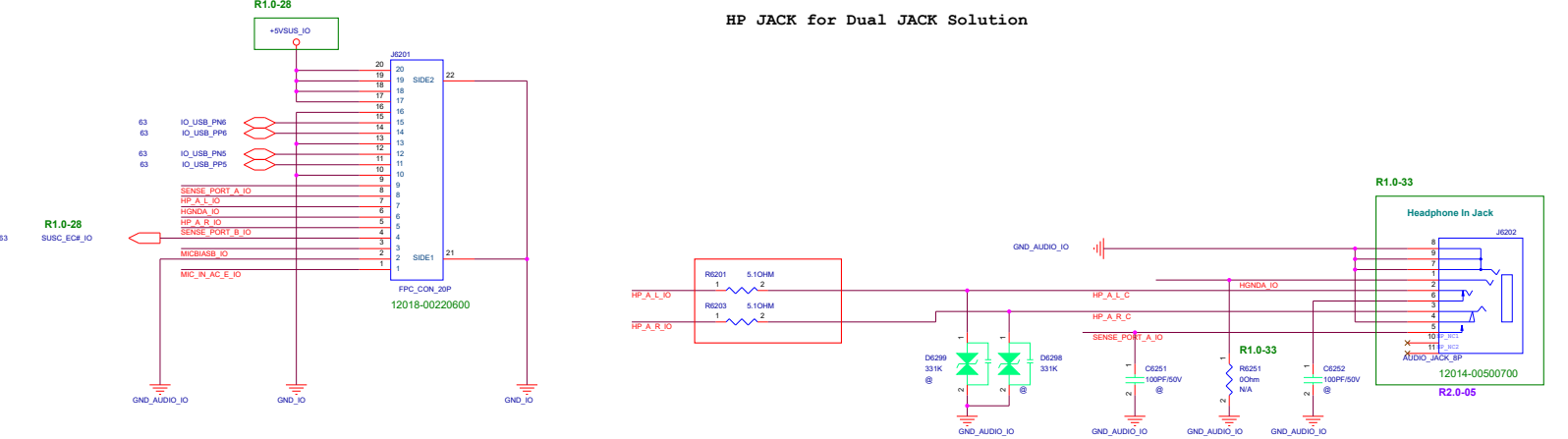
Title : BT_Bluetooth

ASUSTeK COMPUTER

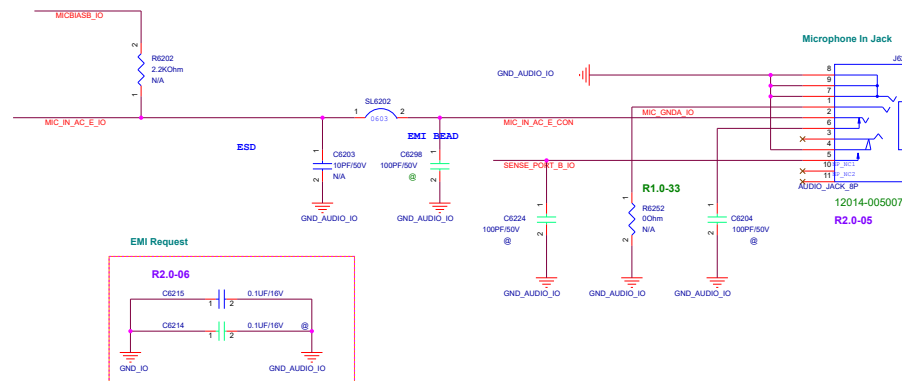
Engineer: Wendell_Lo

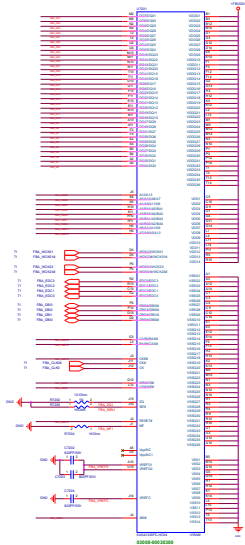
Size	Project Name	Rev
A	GL752VW	1.0

HP JACK for Dual JACK Solution



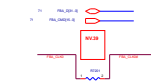
EXTERNAL MICROPHONE





GDD5 MODE SELECTION

MODE	HF	EXS	EXS2
x35	0	0	V000
x32	0	V000	V000
x36 normal	V000	V000	0
x33 normal	V000	V000	V000



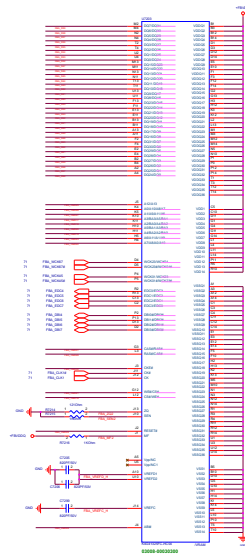
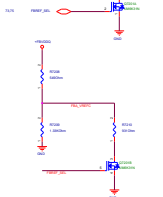
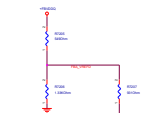
USE GOOD VRAM 128MB x 32 (512MB)

1x1 Pin: 82088-00030900 HYNDX-HSGC-4H24AJR-T2C(A-die) ,Strap: 0x8 (+1.20V)

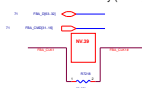
2nd: P/N: 03008-00830400 Micron/EDW0228A80 48-F (A-die), Strap: 8x4 (+1.20V)

3rd PIN: 03008-00030300 SAMSUNGK4041325FC-W004, Straps: 8x3 (+1.5V, non-RV).

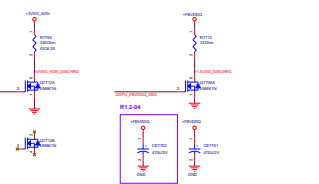
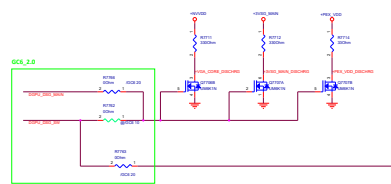
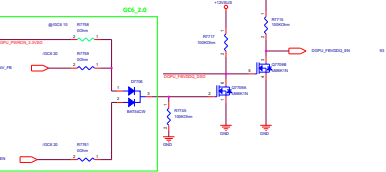
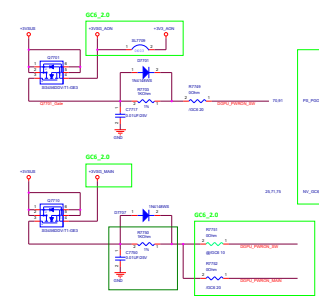
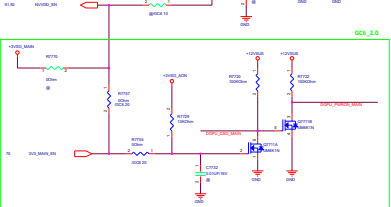
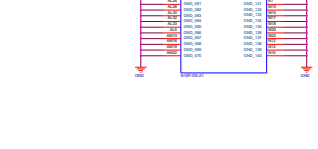
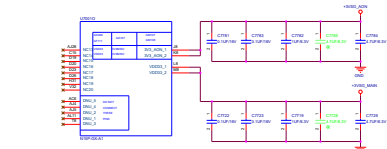
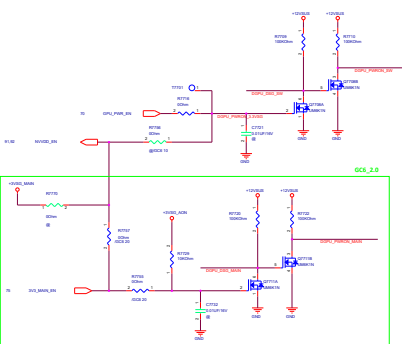
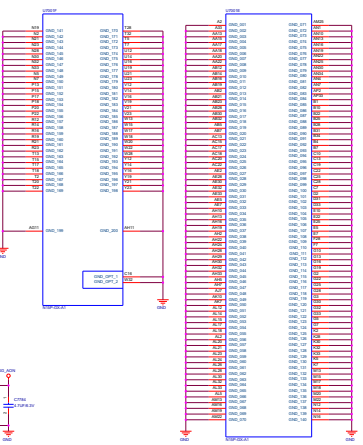
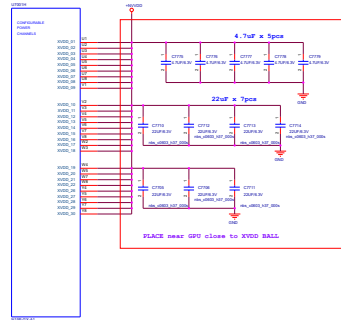
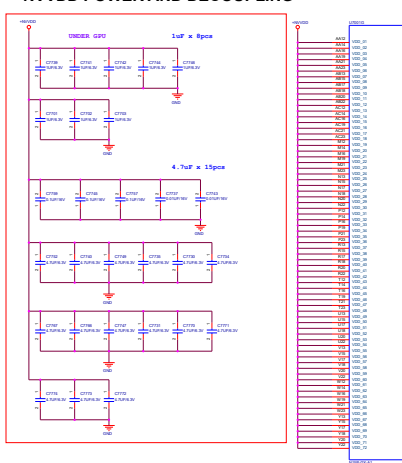
	90010
+1.37V	8.06Kohm
+1.5V	10Kohm



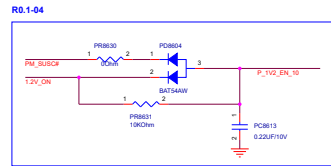
FBA Partition Memory (2 of 2)



NVDD POWER AND DECOUPLING

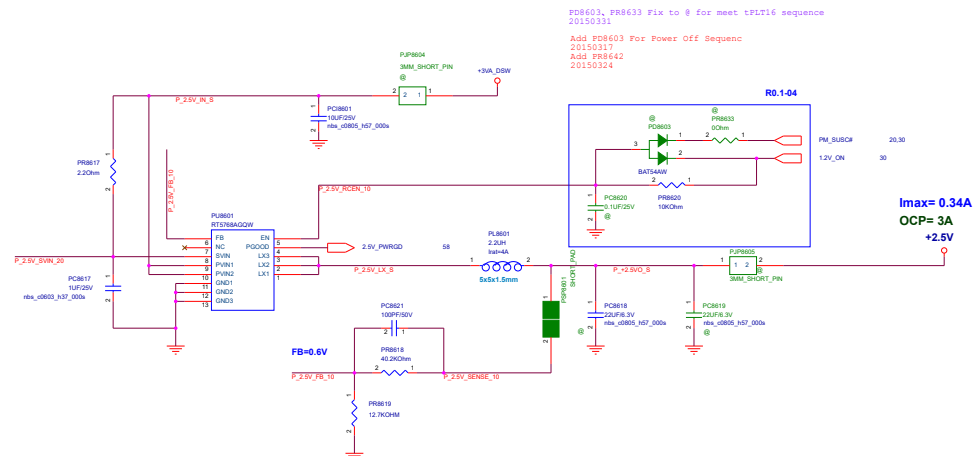
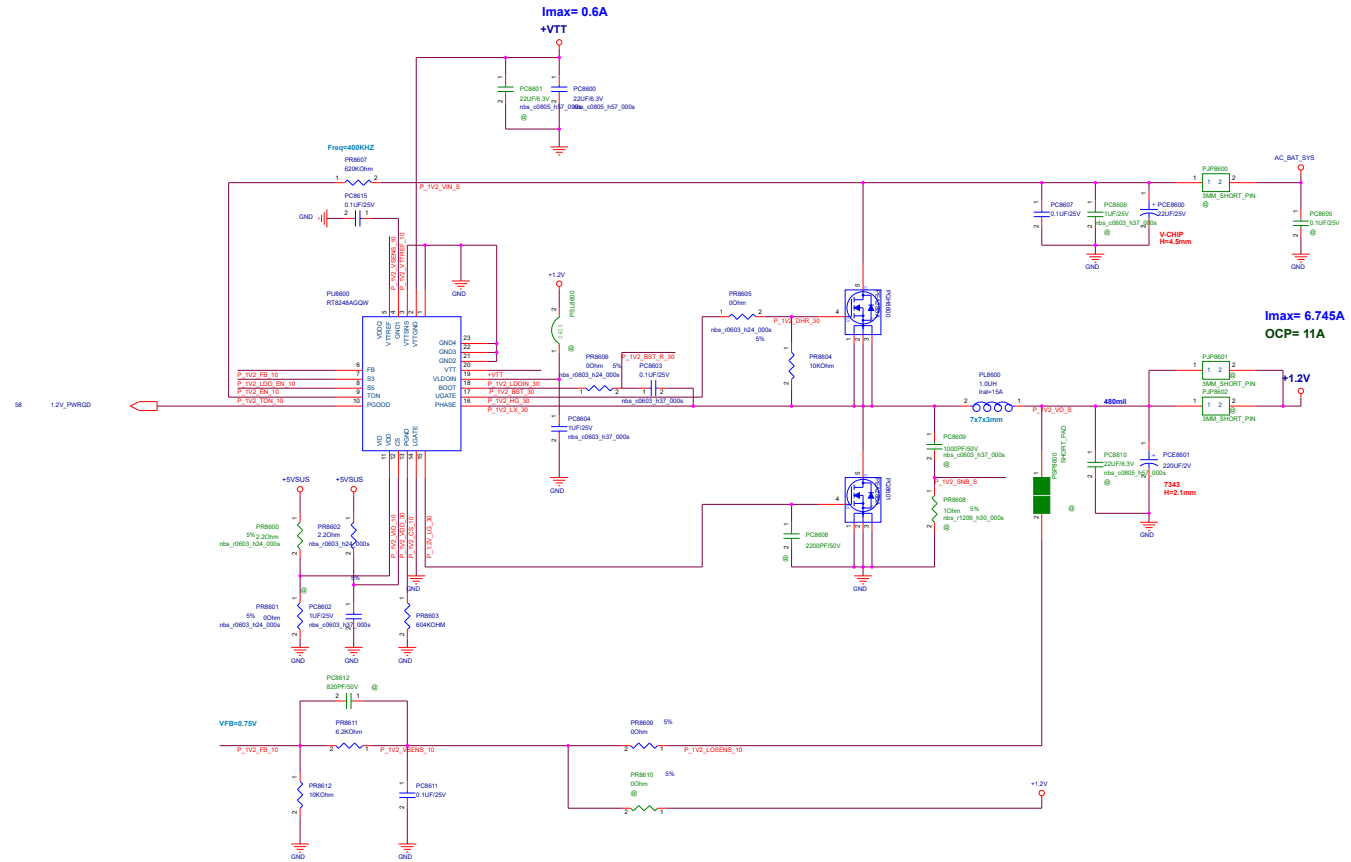
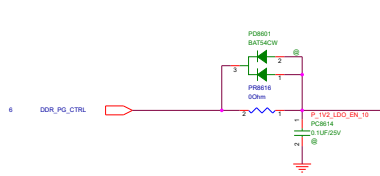


+1.2V / VTT / 2.5V[For Memory]

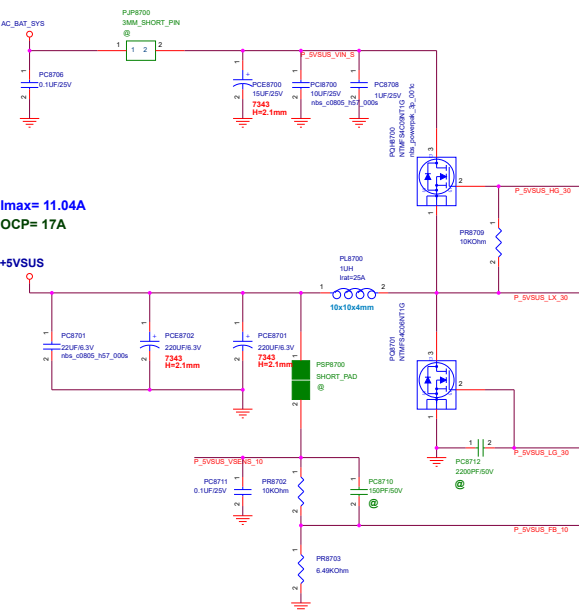


```
Add PD8604 For Power Off Sequence
20150317
Add FR8641
20150324

PC8613 Fix to 0.22uF
延遲1.2V ON, 為確保2.5V比1.2V早Ready
20150331
```



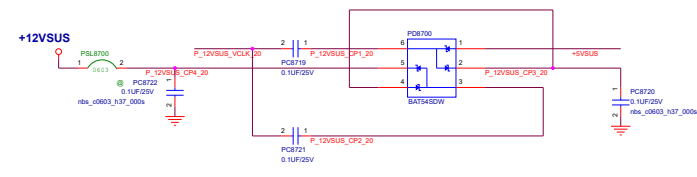
+3VA_DSW / +5VSUS [System Power]



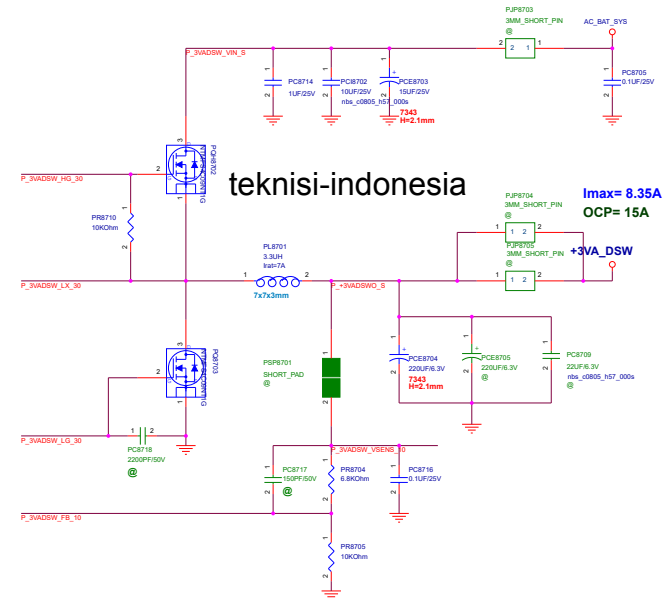
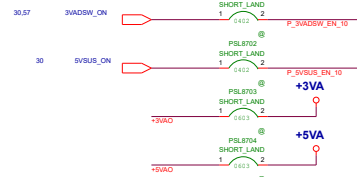
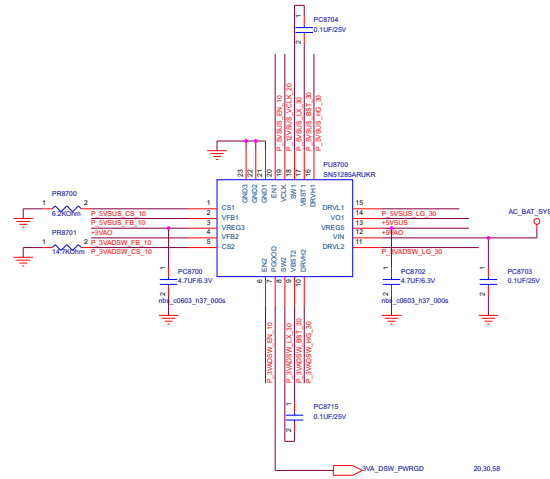
$I_{max} = 11.04A$
OCP= 17A

+5VSUS

+12VSUS



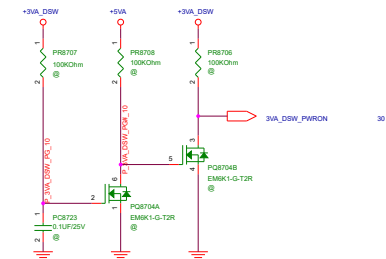
請 check 整份線路 +12VSUS total 並聯對地電阻不得小於10kOhm



teknisi-indonesia

$I_{max} = 8.35A$
OCP= 15A

+3VA_DSW



Adaptor Mode (MVP8)						
	S0	C5	D53	S4	S5	S5 with USB Charger+
PS_ON	1	-	1	-	-	1
3VADSW_ON	1	-	1	-	-	1
3VSUS_ON	1	-	1	-	0	1
5VSUS_ON	1	-	1	-	1	1
1.35V_ON	1	-	1	-	0	0
SUSC_EC#	1	-	1	-	0	0
SUSB_EC#	1	-	0	-	0	0

Battery Mode (MVP8)						
	S0	C5	D53	S4	S5	S5 with USB Charger+
PS_ON	1	-	-	1	0	0
3VADSW_ON	1	-	-	1	0	0
3VSUS_ON	1	-	-	0	0	0
5VSUS_ON	1	-	-	1	0	0
1.35V_ON	1	-	-	1	0	0
SUSC_EC#	1	-	-	0	0	0
SUSB_EC#	1	-	-	0	0	0

